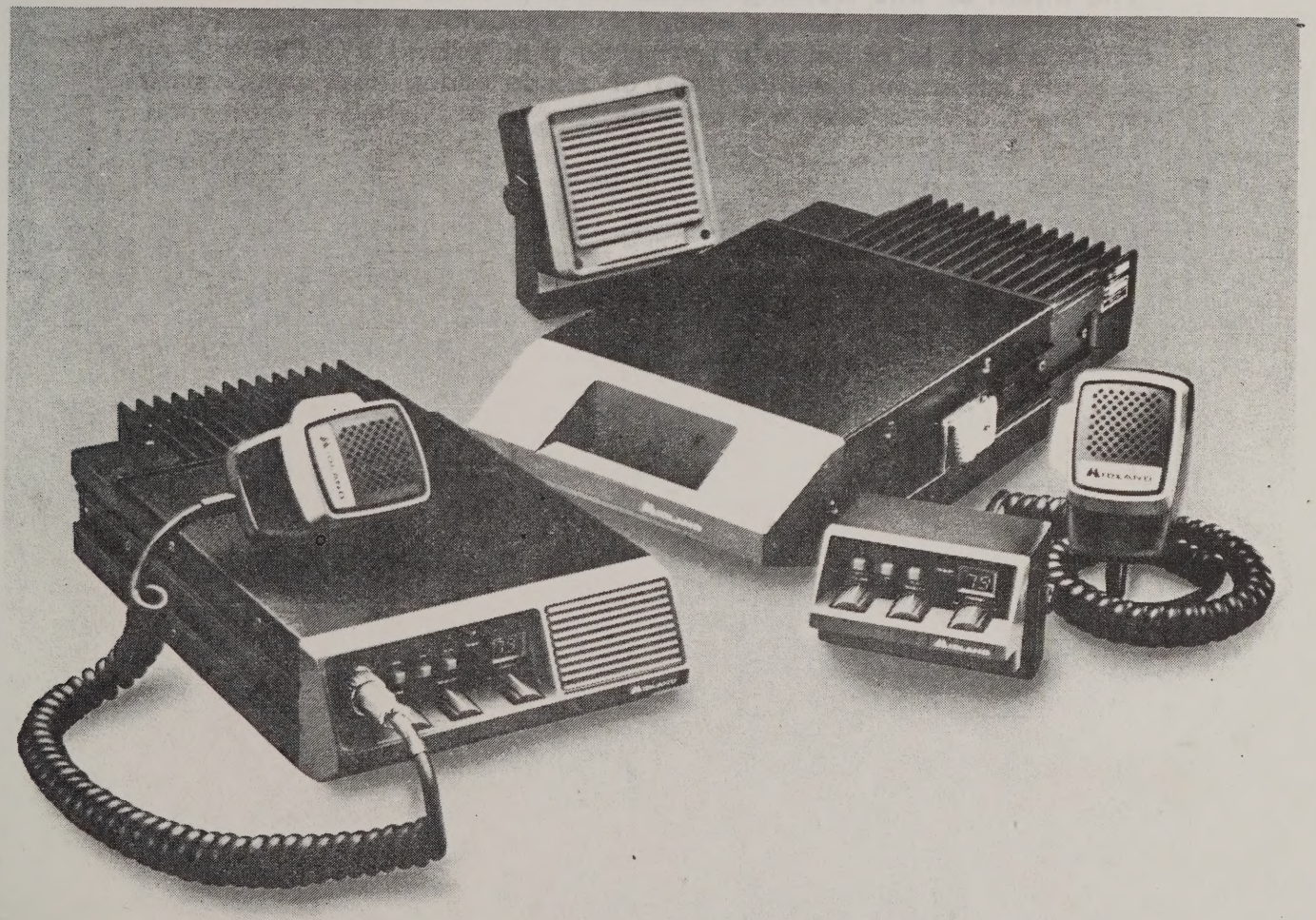
MIDLAND SYN-TECH™

SERVICE TRAINING MANUAL



MIDLAND LMR
LAND MOBILE RADIO
1690 North Topping Avenue
Kansas City, Missouri 64120

05-TM-1/86-5C

INTRODUCTION

The Midland SYNTECH Service Training Manual is designed to be used in conjunction with the Midland SYNTECH Service Manuals. The information contained in this training manual is valid for all frequency ranges of SYNTECH base station and mobile transceivers.

The information given in this training manual will be broken down into several catagories; Theory of operation, schematics, block diagrams, voltage charts, troubleshooting charts. See the table of contents for specific reference to information contained in this training manual.

The intent of this training manual is to provide a qualified technician adequate technical information on the Midland SYNTECH line of base stations and mobile transceivers in order to properly maintain the radios so they will meet or exceed published specifications.

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SYN-TECH SERVICE TRAINING MANUAL

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PERFORMANCE SPECIFICATIONS

GENERAL SPECIFICATIONS:

Nominal Operating Voltage		13.6 VDC negative gnd.
Temperature Range		-30 C to +60 C
Antenna Impedance		50 ohms, unbalanced
Microphone		Dynamic, with amplifier
Speaker		Internal 8 ohms External 4 ohms
Frequency Control		Synthesized with EPROM
Frequencies of Operation	Low Band	29 - 54 MHz
	Mid Band	66 - 88 MHz
	VHF Band	136 - 174 MHz
	UHF Band	406 - 512 MHz
	800 MHz	806 - 866 MHz
Performance Bandwith	Low Band	TX - 1 MHz RX - 1 MHz
	Mid Band	TX - 2 MHz RX - 2 MHz
	VHF Band	TX - 4.5 MHz RX - 4.5 MHz
	UHF Band	TX - 10 MHz RX - 5 MHz
	800 MHz	TX - 60 MHz RX - 5 MHz
Frequency Tolerance and Stability	800 MHz	2.5 PPM
	Others	5.0 PPM
Channel Capability		80 Channels TX and RX
Current Drain		See specific service manual for specific model.

PERFORMANCE SPECIFICATIONS

RECEIVER SPECIFICATIONS:

Senstivity	12 DB SINAD	.25uV @ 50 ohm
Squelch Senstivity	Threshold	.2uV max or 6dB SINAD
	Tight	1.0uV min, 2.0uV max
Receiver Attack (squelch release) time	100ms max	
Receiver Squelch Closing Time	200ms max	
Modulation Acceptance Bandwidth	±7.0KHz min @ 20/25/30 KHz ±4.5KHz min @ 12.5 KHz	
Adjacent Channel Two Signal Selectively and Desensitization	Low Band	90dB @ ±20KHz
	Mid Band	90dB @ ±30KHz
	VHF Band	90dB @ ±30KHz
	UHF Band	90dB @ ±25KHz
	800 MHz	75dB @ ±25KHz
Spurious Responce Attenuation	800 MHz	85dB
	all others	90dB
Intermodulation Spurious Responce Attenuation. Measured at usable sensitivity.	Low Band	90dB
	Mid Band	80dB
	VHF Band	80dB
	UHF Band	80dB
	800 MHz	75dB
Audio Power Output	1W @ 5% THD @ 8 ohms	Internal
	5W @ 5% THD @ 4 ohms	External
Hum and Noise	Unsquelched	40dB
	Squelched	50dB
Conducted Spurious RF power	200 uV across 50 ohms (800pW) from DC to 1000 MHz	
Intermediate Frequencies	Low Band	10.7 MHZ 1st, 455KHz 2nd
	Mid Band	21.4 MHz 1st, 455KHz 2nd
	VHF Band	21.4 MHz 1st, 455KHz 2nd
	UHF Band	21.4 MHz 1st, 455KHz 2nd
	800 MHz	47.0 MHz 1st, 455KHz 2nd

PERFORMANCE SPECIFICATIONS

TRANSMITTER SPECIFICATIONS:

Carrier Power Output	30 Watt Models	15 - 30 Watts
	40 Watt Models	20 - 40 Watts
	50 Watt Models	25 - 50 Watts
	65 Watt Models	40 - 65 Watts
	80 Watt Models	40 - 80 Watts
	110 Watt Models	50 - 110 Watts
	15 Watt Models	5 - 15 Watts
	35 Watt Models	20 - 35 Watts
Modulation System	Phase Modulation	PM
Audio frequency harmonic distortion	3% @ 1000 Hz for ±3.0 KHz deviation	
System Deviation	±5KHz max	
Modulation limiting	Instantaneous peak clipping with low pass audio filter	
Hum and Noise	50dB	
Transmitter carrier attack time	100ms max for 50% rated power	
Conducted spurious emissions	Less than 25uW, 1MHz to 1000MHz	
Microphone input level and impedance	-8dbm ±3db/600 ohms	
Output protection	Shall withstand for 5 minutes all VSWR around Smith Chart of 20:1 without failure or damage	
Output stability	Shall not exceed spurious emission requirements when operated into a mis-match load with 5:1 VSWR at any point on the Smith Chart	

PERFORMANCE SPECIFICATIONS

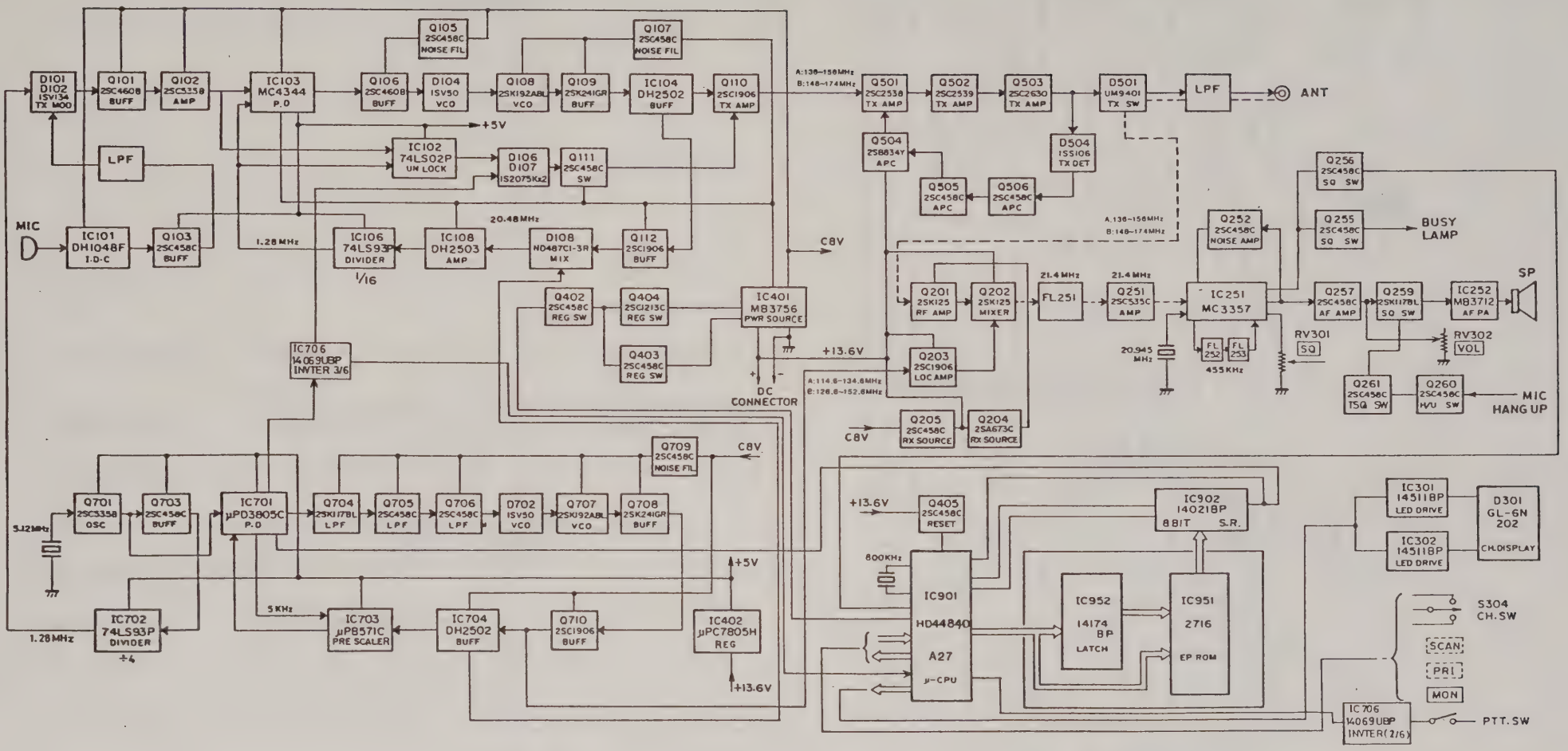
SCAN SPECIFICATIONS:

Scan Speed	20 Channels/second
Channel Capacity	64 (PRI) 64 (SCAN)
Scan Detection	Carrier, tone or vacant channel
Scan Resume Delay	0.3/2.5/5.0 or inifinite seconds

CTCSS SPECIFICATIONS:

Code Frequencies	All EIA standard from 67Hz to 241.8Hz
Modulation Limits	500 - 1000 MHz
Decode Sensitivity	Less than 5db SINAD
Receiver Responce Time	200ms max
Encode Responce Time	50ms max
Transmitter Tone Distortion	5% max
Transmitter Intermodulation Distrotion	10%

BLOCK DIAGRAM



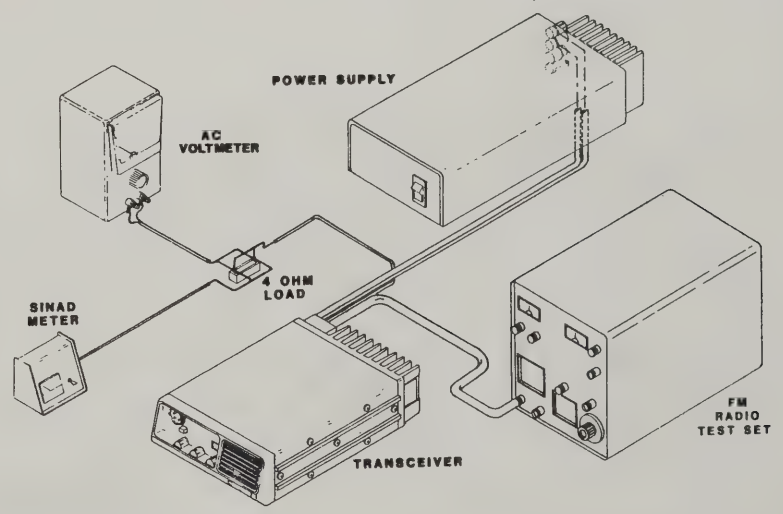
SUGGESTED TEST INSTRUMENTS

TEST INSTRUMENT	REQUIRED SPECIFICATIONS	INSTRUMENT TYPE
DC Power Supply	13.8 VDC 10amps	Power/Mate BPA-20F
Watt Meter	136-174 MHz	Bird Model 43 with 50C Element and 50 watt, 50 ohm load
Digital Multimeter	AC 100 mv - 10v DC 100 mv - 100v	B-K 2810
AC Voltmeter	10mv - 10v	Heath SM-5238
Speaker Load	4 ohm speaker and resistive load (switchable)	Shop Fabricated
RF Signal Generator	136-174 MHz Range. Calibrated output 0.1 to 100 uV. Internal and external modulation capability with internal frequency of 1 KHz at 5 KHz deviation.	Cushman CE-31A
Deviation Meter	0 - 5 KHz Deviation Range +/- Deviation Capability	Cushman CE-31A
Frequency Meter	Frequency Range 136-174 MHz Frequency tolerance of +/- .00002%	Cushman CE-31A or Heath SM-4120
Signal Generator	0-10 KHz Sine Wave 0-5V	Heath SG-5218
LMR Test Set	- - - - - - - - - - - - - - - - - -	Midland 70-E10
Sinad Meter	- - - - - - - - - - - - - - - - - -	Helper Instruments Sinadder

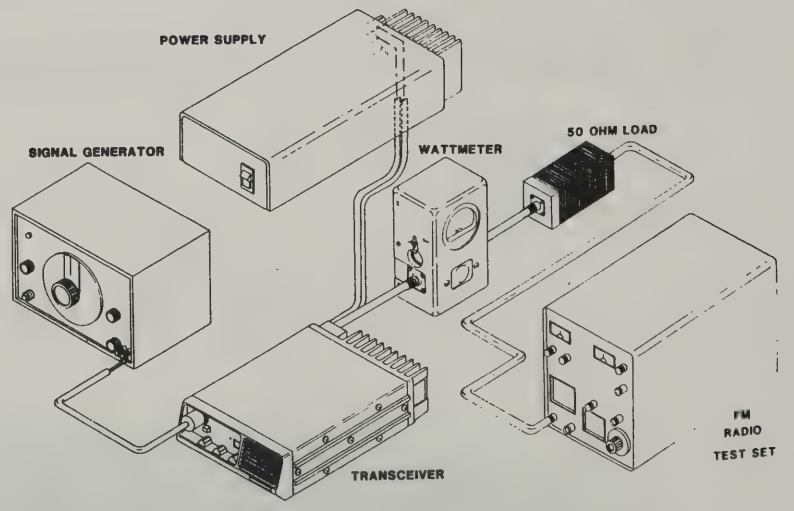
Fold Out

TEST EQUIPMENT SET-UP DIAGRAMS

RECEIVER TEST SET-UP



TRANSMITTER TEST SET-UP



POWER SUPPLY

THEORY OF OPERATION:

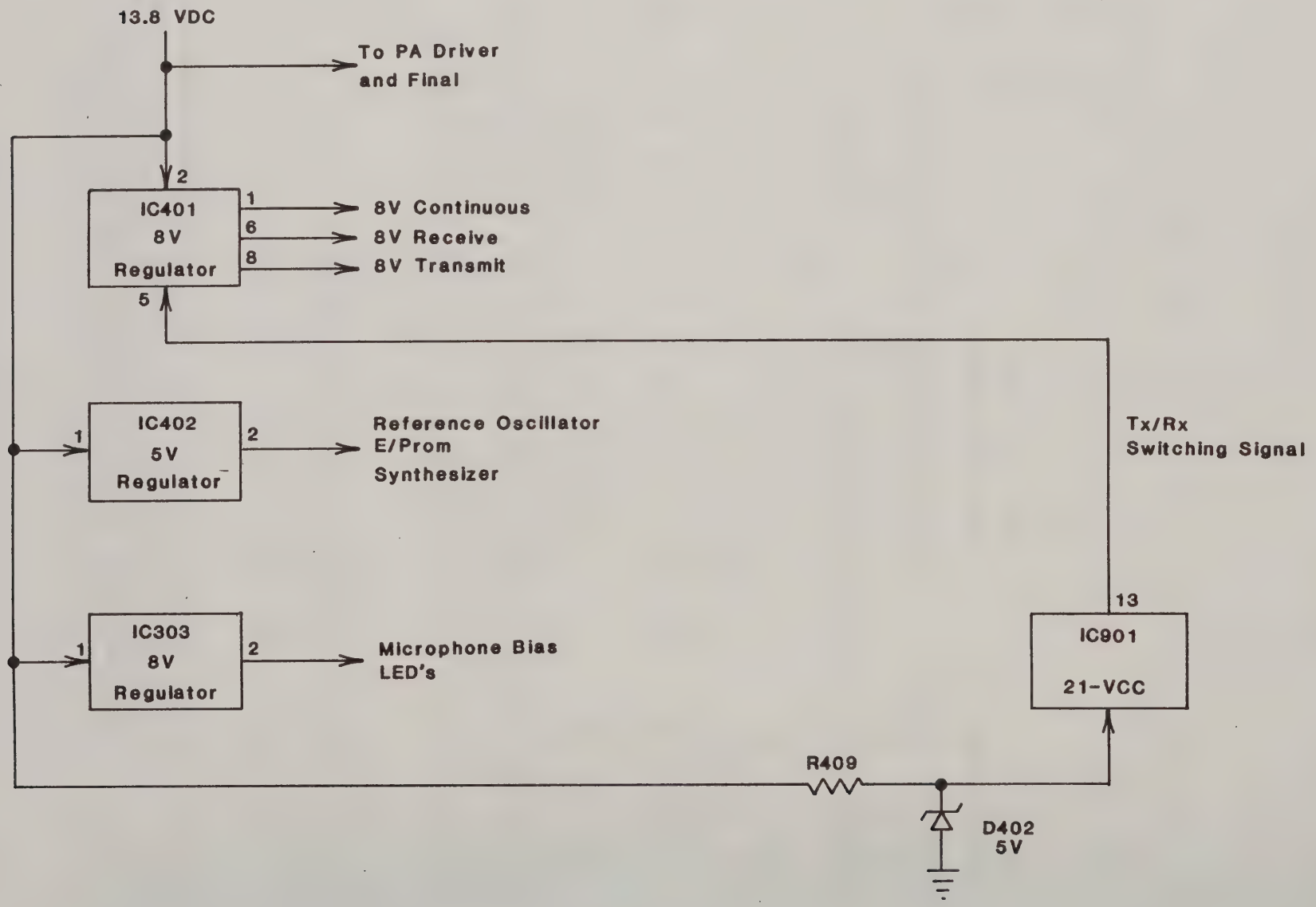
The 13.6 VDC input is filtered by L256 and related components and switched by K201 (trunk-mount models) or the unit on-off switch (under-dash models). This filtered 13.6 VDC is supplied directly to the PA driver and final stages and also to pin 2 of IC401, the main voltage regulator. IC401 outputs a constant 8 VDC from pin 1 as well as 8 VDC during receive from pin 8 and 8 VDC during transmit from pin 6. The receive/transmit switching signal is output from IC901 pin 13 through Q402 and Q403 to IC401 pin 5. Regulator IC402 (Tx board) provides 5 VDC for the reference oscillator, synthesizer integrated circuits and the E/PROM module. Regulator IC303 (control panel or control head) supplies 8 VDC for microphone bias and LED displays. The microcomputer IC901 is supplied 5 VDC from zener diode D402, which is powered by an unswitched 13.6 VDC source. This allows the microcomputer to retain memory of the last selected channel as long as power is connected to the radio. Other microcomputer functions are disabled at unit turn-off, since power is removed from pin 19, the standby control pin.

VOLTAGE CHARTS:

ANALOG IC

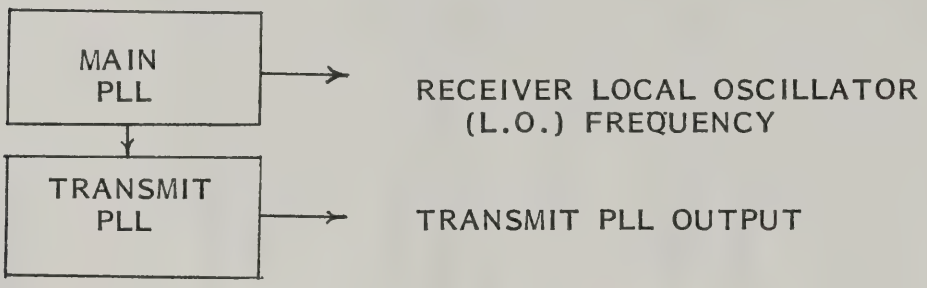
REF.NO.	DESCRIPTION	MODE	PIN No.1	PIN No.2	PIN No.3	PIN No.4	PIN No.5	PIN No.6	PIN No.7	PIN No.8	PIN No.9	PIN No.10	PIN No.11	PIN No.12					FUNCTION
IC 303	uPC7808H	TX	13.8	8.0	0	--	--	--	--	--	--	--	--	--					POWER REGULATOR
		RX	13.8	8.0	0	--	--	--	--	--	--	--	--	--					
IC 401	MB 3756	TX	8.0	13.6	8.0	0	0	0	0	8	--	--	--	--					POWER REGULATOR
		RX	8.0	13.6	8.0	0	1.7	8	0	0	--	--	--	--					
IC 402	uPC7805H		13.8	0	4.9														POWER REGULATOR

POWER SUPPLY BLOCK DIAGRAM



PLL/SYNTHESIZER FUNCTION

The frequency synthesizer consist of two phased-locked loops. One loop (Main PLL) is controlled directly by the microcomputer and generates the receive local oscillator frequency. This loop also generates a frequency used in the second loop (Transmit PLL) for transmitter operation.



Radio Frequency Range		RX L.O. Frequency	TX PLL Output
Low Band	A Band	39.7 - 47.7 MHz	29 - 37 MHz
	B Band	45.7 - 54.7 MHz	35 - 44 MHz
	C Band	50.7 - 64.7 MHz	40 - 54 MHz
Mid Band	A Band	87.4 - 98.4 MHz	66 - 77 MHz
	B Band	98.4 - 109.4 MHz	77 - 88 MHz
VHF Band	A Band	114.6 - 134.6 MHz	136 - 156 MHz
	B Band	126.6 - 152.6 MHz	148 - 174 MHz
UHF Band	A Band	384.6 - 408.6 MHz	406 - 430 MHz
	B Band	428.6 - 448.6 MHz	450 - 470 MHz
	C Band	448.6 - 472.6 MHz	470 - 494 MHz
	D Band	472.6 - 490.6 MHz	494 - 512 MHz
	E Band	408.6 - 428.6 MHz	430 - 450 MHz
800 MHz		759.0 - 819.0 MHz	806 - 866 MHz

REFERENCE OSCILLATOR AND MAIN PLL

A stable frequency for the entire radio is generated by a crystal oscillator composed of X101, Q701 and related components. The stability of this oscillator is maintained by use of a positor crystal heater. This oscillator operates at the frequencies listed below for the different frequencies of SYNTECH radios.

Low Band - 5.12 MHz
Mid Band - 5.12 MHz
VHF Band - 5.12 MHz
UHF Band - 12.8 MHz
800 Mhz - 12.8 MHz

The main oscillator frequency is divided by 1024 in IC701 to generate a reference frequency for the Main PLL loop which consist of IC701 (phase comparator and programmable divider), Q704-706 (loop low pass filter), D702/Q707 (VCO), IC704 (VCO for 800 MHz models), and IC703 (pre-scaler). The reference frequencies generated for each frequency range of SYNTECH radios is listed below.

Low Band - 5.0 KHz
Mid Band - 5.0 KHz
VHF Band - 5.0 KHz
UHF Band - 12.5 KHz
800 MHz - 12.5 KHz

The Main VCO frequencies produced for each frequency range of SYNTECH radio is calculated as follows.

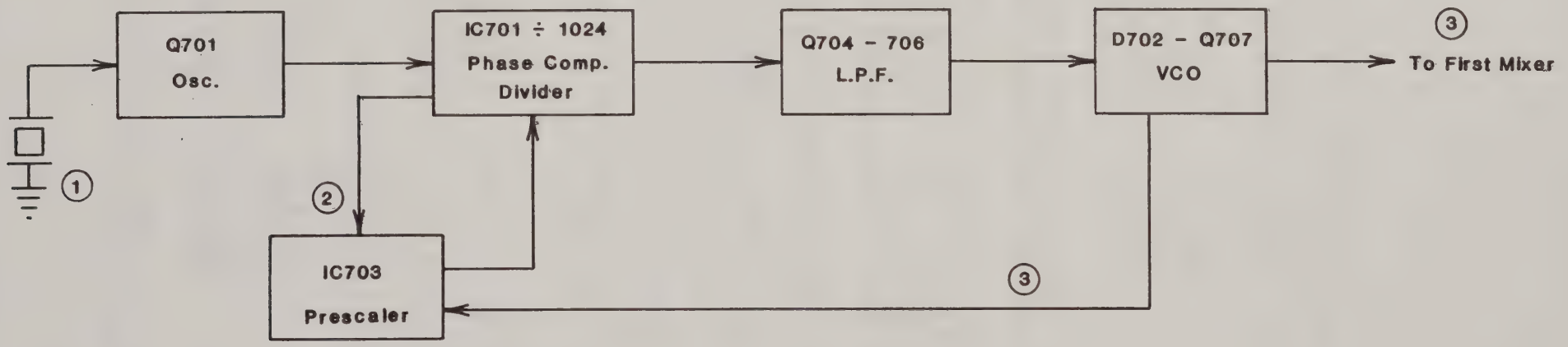
FREQUENCY RANGE	RECEIVER VCO FREQUENCY	TRANSMIT VCO FREQUENCY
Low Band	FRX + 10.7 MHz	FTX + 10.24 MHz
Mid Band	FRX + 21.4 MHz	FTX + 20.48 MHz
VHF Band	FRX - 21.4 MHz	FTX - 20.48 MHz
UHF Band	FRX - 21.4 MHz	FTX - 19.20 MHz
800 MHz Band	FRX - 47.0 MHz	FTX - 19.20 MHz

The Main VCO frequency is divided by the ratios listed below,

Low Band - 32/33
Mid Band - 32/33
VHF Band - 64/65
UHF Band - 64/65
800 MHz - 64/65

by pre-scaler IC703 and further divided in IC701. The divison ratio of IC701 is controlled by the 8 bit code latched into the shift register IC902 from the EPROM IC951 under control of the microcomputer IC901. The 8 bit code is sent in serial fashion from IC902 to IC701 under microcomputer control. Besides being a programmable divider, IC701 is also a phase comparator which generates an error signal for VCO control if the programmable divider output is out of phase with the 5 KHz signal generated in the low band, mid band and VHF band radios; and 12.5 KHz in the UHF band and 800 MHz radios.

MAIN PLL & REFERENCE OSCILLATOR BLOCK DIAGRAM



①

LOW BAND - 5.12 MHz
MID BAND - 5.12 MHz
VHF BAND - 5.12 MHz
UHF BAND - 12.8 MHz
800MHz - 12.8 MHz

②

LOW BAND - 5.0 KHz
MID BAND - 5.0 KHz
VHF BAND - 5.0 KHz
UHF BAND - 12.5 KHz
800MHz - 12.5 KHz

③

LOW BAND	A BAND - 39.7 - 47.7 MHz
	B BAND - 45.7 - 54.7 MHz
	C BAND - 50.7 - 64.7 MHz
MID BAND	A BAND - 87.4 - 98.4 MHz
	B BAND - 98.4 - 109.4 MHz
VHF BAND	A BAND - 114.6 - 134.6 MHz
	B BAND - 126.6 - 152.6 MHz
UHF BAND	A BAND - 384.6 - 408.6 MHz
	B BAND - 428.6 - 448.6 MHz
	C BAND - 448.6 - 472.6 MHz
	D BAND - 472.6 - 490.6 MHz
	E BAND - 408.6 - 428.6 MHz
800MHz	759.0 - 819.0 MHz

MODULATOR AND TRANSMIT PLL

The main reference oscillator frequency, which operates at the frequencies listed below,

Low Band	-	5.12 MHz
Mid Band	-	5.12 MHz
VHF Band	-	5.12 MHz
UHF Band	-	12.8 MHz
800 MHz	-	12.8 MHz

is also fed to IC702 (4 bit binary counter) where is is divided by

Low Band	-	8	640 KHz
Mid Band	-	4	1.28 MHz
VHF Band	-	4	1.28 MHz
UHF Band	-	8	1.60 MHz
800 MHz	-	8	1.60 MHz

to generate a new frequency listed in the table above. This new frequency goes directly to the transmit phase shift modulator D101/ D102. Audio from the microphone is shaped and limited by IC101 (instantaneous deviation control), filtered and buffered and fed to the phase shift modulator. The modulated outpur becomes the reference frequency for the transmit PLL loop consisting of IC103 (phase comparator), D104/Q108 (VCO), IC104 (VCO for 800 MHz models), D108 (mixer), and IC106 (fixed divider). The VCO output is at the transmit channel frequency and is mixed at D108 with the frequencies listed below from the Main PLL loop

Low Band	-	FTX + 10.24 MHz
Mid Band	-	FTX + 20.48 MHz
VHF Band	-	FTX - 20.48 MHz
UHF Band	-	FTX - 19.20 MHz
800 MHz	-	FTX - 19.20 MHz

to yield the transmitter IF frequencies listed below for the different frequency ranges of SYNTECH radios.

Low Band	-	10.24 MHz
Mid Band	-	20.48 MHz
VHF Band	-	20.48 MHz
UHF Band	-	19.20 MHz
800 MHz	-	19.20 MHz

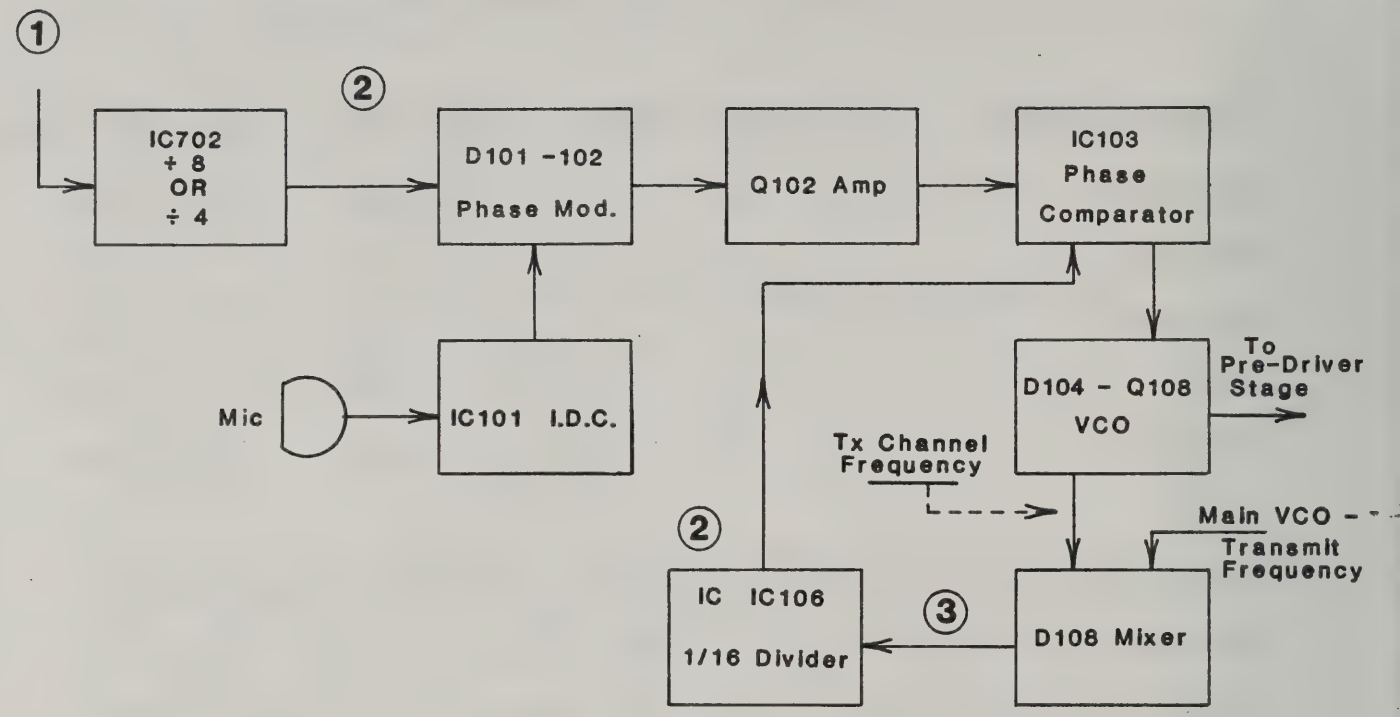
This frequency is divided in IC106 to give a new frequency, and is compared with the reference signal from the modulator. The division ratio of IC106, the new frequency and the modulator reference frequency are listed in the chart below.

MODULATOR AND TRANSMIT PLL

Frequency Range	IC106 Division Ratio	New Freq.	Mod. Ref. Freq.
Low Band	16	640 KHz	640 KHz
Mid Band	16	1.28 MHz	1.28 MHz
VHF Band	16	1.28 MHz	1.28 MHz
UHF	12	1.60 MHz	1.60 MHz
800 MHz	12	1.60 MHz	1.60 MHz

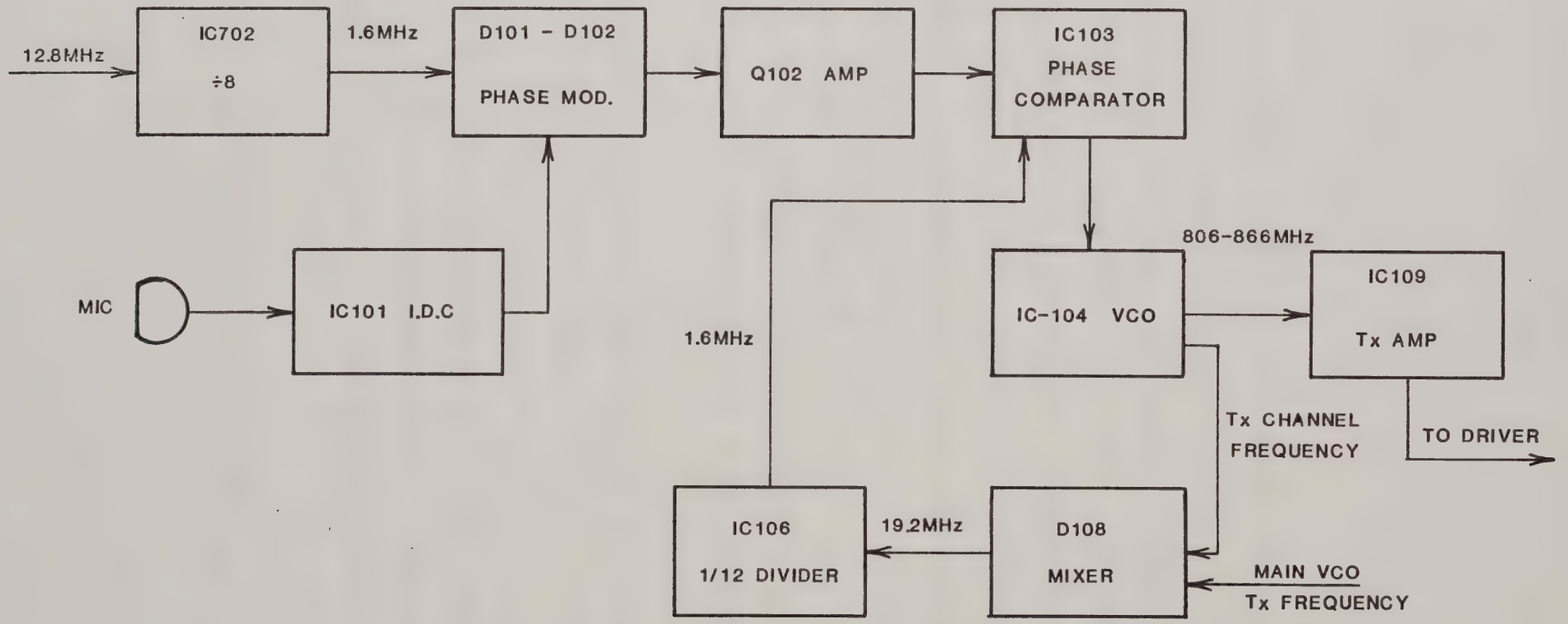
Thus the VCO output is forced to track the modulated reference signal, reproducing this modulation at the transmit frequency. IC102 detects any large differences between the two phase comparator inputs and generates an out-of-look signal which biases Q111 on in the Low Band, Mid Band, VHF Band, and UHF Band radios. With Q111 biased on, the transmitted signal is prevented from reaching the final stages of the radio. In the 800 MHz radios, the out-of-lock signal biases Q108 off through Q111, Q112 and Q109. This prevents any transmitter signal from reaching the power amplifier stages. Q111 is biased on (Q108 biased off) during receive by a signal from the microcomputer IC901 pin 6.

TRANSMITTER BLOCK DIAGRAM



①	②	③
LOW BAND - 5.12 MHz	LOW BAND - 640 KHz	LOW BAND - 10.24 MHz
MID BAND - 5.12 MHz	MID BAND - 1.28 MHz	MID BAND - 20.48 MHz
VHF BAND - 5.12 MHz	VHF BAND - 1.28 MHz	VHF BAND - 20.48 MHz
UHF BAND - 12.8 MHz	UHF BAND - 1.60 MHz	UHF BAND - 19.20 MHz

TRANSMITTER BLOCK DIAGRAM - 800MHz

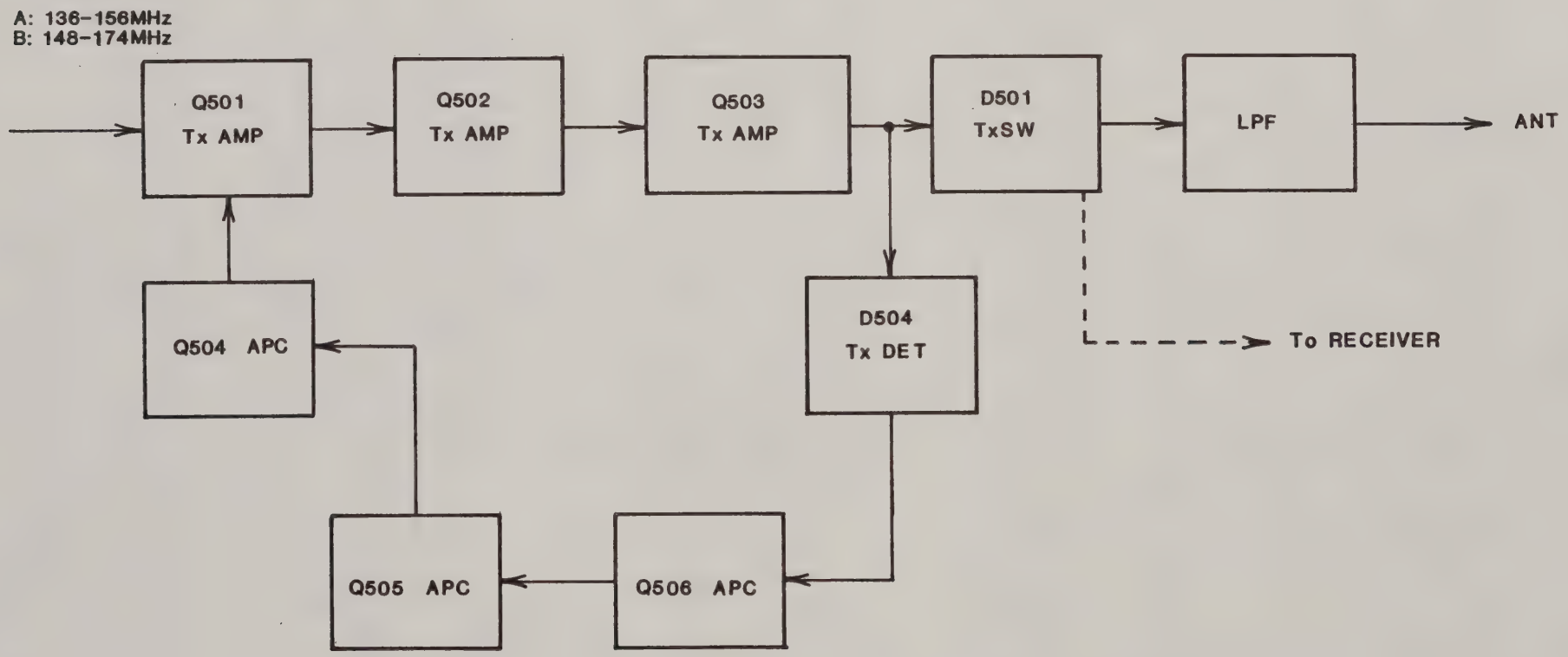


TRANSMIT POWER AMPLIFIER AND APC (AUTOMATIC POWER CONTROL)

For instructional purposes, we will discuss the power amplifier and automatic power control circuitry for the 40 watt VHF band SYN-TECH transceiver. The other frequency ranges of SYN-TECH radios and the higher power VHF band radios operate on these same basic principles. For a thorough discussion on the transmit power control circuitry of these radios, please see the specific service manual for this information.

The transmit PLL output is amplified by Q110 before being fed to the PA section. The Q110 output is amplified to rated power by Q501 (pre-driver), Q502 (driver), and the final transistor Q503. A sample of the RF output is detected by D504 and coupled to the differential amplifier Q506/Q505. The output of Q505 controls the conduction of Q504 which in turn controls the gain of the pre-driver Q501. Thus any changes in output power are automatically corrected by this control loop. Output power is set at alignment by RV502. Transmitter harmonics are eliminated by output low pass filtering composed of L512-L515 and C525-C529. The PIN diode switch D501 is biased to a low resistance state during transmit and a high impedance condition during receive.

SYN-TECH 70-340 VHF 40 WATT POWER AMPLIFIER



RECEIVER RF/IF/DETECTOR

The theory of operation for the RF, IF and detector sections will be broken down into three sections. The first section will cover the low band, mid band and VHF transceivers. The second section will cover the UHF transceiver and the third section will cover the 800 MHz transceiver.

LOW BAND - MID BAND - VHF

The receiver front end consist of filtering by C201-C206 and L201-L203 and RF amplification by Q201. After further filtering the RF signal is mixed at the FET mixer Q202 with the local oscillator signal generated by the Main PLL loop to give the first IF frequency. The local oscillator frequency and first IF frequency for the low band, mid band and VHF radios is given in the chart below.

MODEL		RX LOCAL OSC. FREQ.	1st IF FREQ.
Low Band	A Band	39.7 - 47.7 MHz	10.7 MHz
	B Band	45.7 - 54.7 MHz	10.7 MHz
	C Band	50.7 - 64.7 MHz	10.7 MHz
Mid Band	A Band	87.4 - 98.4 MHz	21.4 MHz
	B Band	98.4 - 109.4 MHz	21.4 MHz
VHF Band	A Band	114.6 - 134.6 MHz	21.4 MHz
	B Band	126.6 - 152.6 MHz	21.4 MHz

The IF signal is filtered by the crystal filter FL251, amplified by Q251 and fed to the internal mixer of IC251. The 2nd local oscillator frequency is generated by X251 and the IC251 internal oscillator and injected into the internal mixer, producing the 2nd IF frequency of 455KHz. The 2nd local oscillator frequency for the low band, mid band and VHF band radios is listed below.

MODEL	2nd LOCAL OSCILLATOR FREQUENCY
Low Band	10.245 MHz
Mid Band	20.945 MHz
VHF Band	20.945 MHz

The 2nd IF signal is filtered by FL252 and FL253, amplified and limited by the amplifier/limiter stage of IC251, and injected into the quadrature circuit consisting of L252 and the internal balanced mixer of IC251. The output of the balanced mixer is the detected audio signal.

RECEIVER RF/IF/DETECTOR

UHF BAND

The receiver front end consist of filtering by L201-L202 and RF amplification by Q201 and Q202. After further filtering by L203-L206 the RF signal is mixed at the FET mixer Q203 with the local oscillator signal generated by the Main PLL loop to give the 21.4 MHz IF. The local oscillator frequencies for the different frequency ranges of UHF radios is listed below.

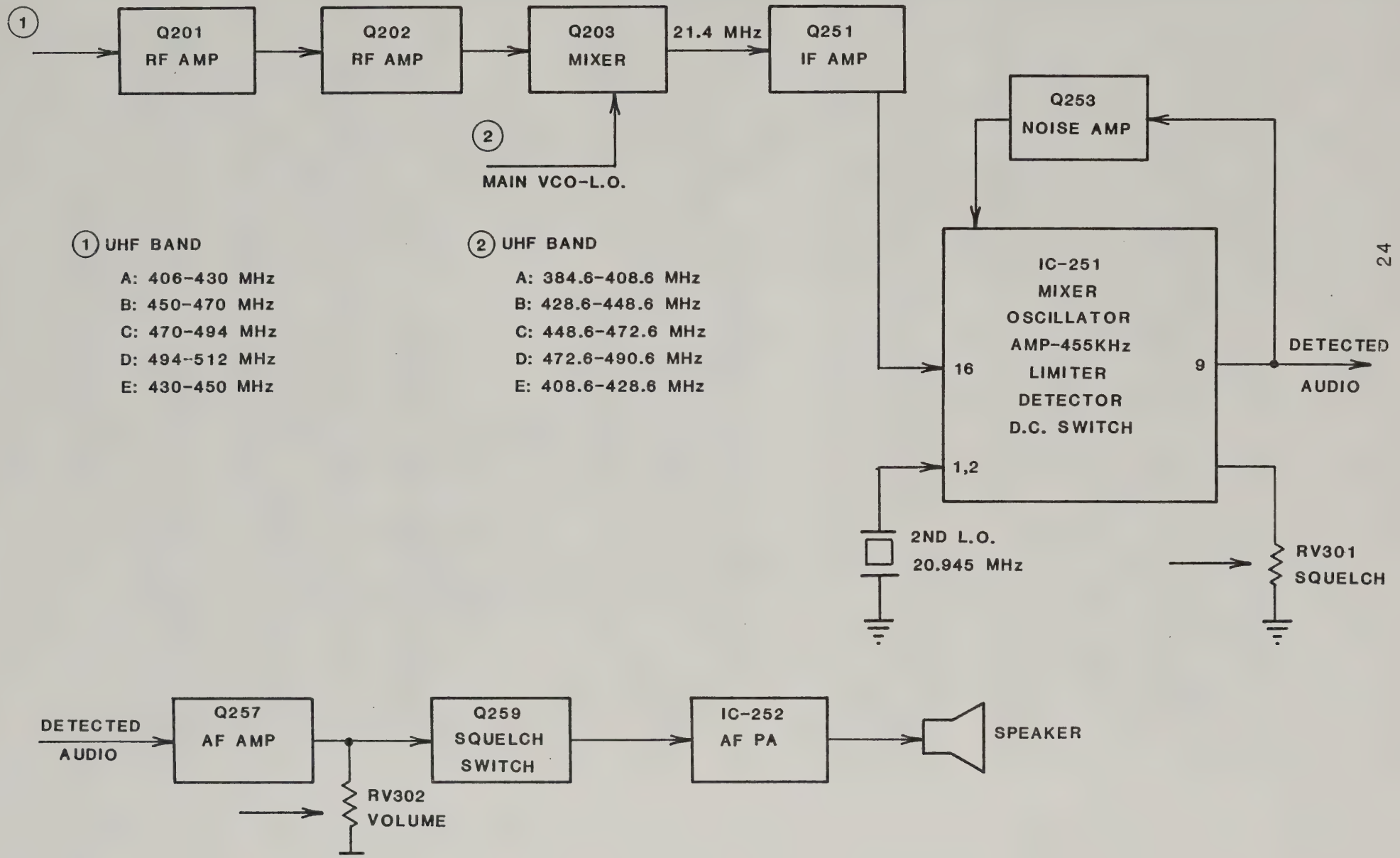
MODEL		RX LOCAL OSCILLATOR FREQUENCY
UHF Band	A Band	384.6 - 408.6 MHz
	B Band	428.6 - 448.6 MHz
	C Band	448.6 - 472.7 MHz
	D Band	472.6 - 490.6 MHz
	E Band	408.6 - 428.6 MHz

The IF signal is filtered by the crystal filter FL251, amplified by Q251 and fed to the internal mixer of IC251. The 2nd local oscillator frequency of 20.945 MHz is generated by X251 and the IC251 internal oscillator and injected into the internal mixer, producing the 2nd IF of 455 KHz. The 2nd IF signal is filtered by FL252 and FL253, amplified and limited by the amplifier-limiter stages of IC251, and injected into the quadrature detector circuit consisting of L252 and the internal balanced mixer of IC251. The output of the balanced mixer is the detected audio signal.

800 MHz BAND

The receiver front end consist of filtering by helical resonators L201-1 and L202-1 and RF amplification by IC201. The RF signal is further filtered by helical resonators L201-2 and L202-2 and coupled to the hybrid mixer composed of IC202 and IC203. The other input to the first mixer is the local oscillator signal generated by the Main PLL loop (759-819 MHz) and amplified by IC204. The first mixer output is at the 47.0 MHz IF frequency and is filtered by crystal filters FL201 and FL202 and coupled to the second mixer Q201. The second local oscillator frequency of 47.455 MHz is generated by X201 and Q202. The 455 KHz second IF signal is filtered by the ceramic filter FL251, amplified by Q251 and fed to IC251 for further amplification, filtering by FL252 and limiting by the amplifier-limiter stages. The resulting limited signal is injected into the quadrature detector circuit consisting of L252 and the internal balanced mixer of IC251. The balanced mixer output is the detected audio signal.

RECEIVER BLOCK DIAGRAM
UHF BAND



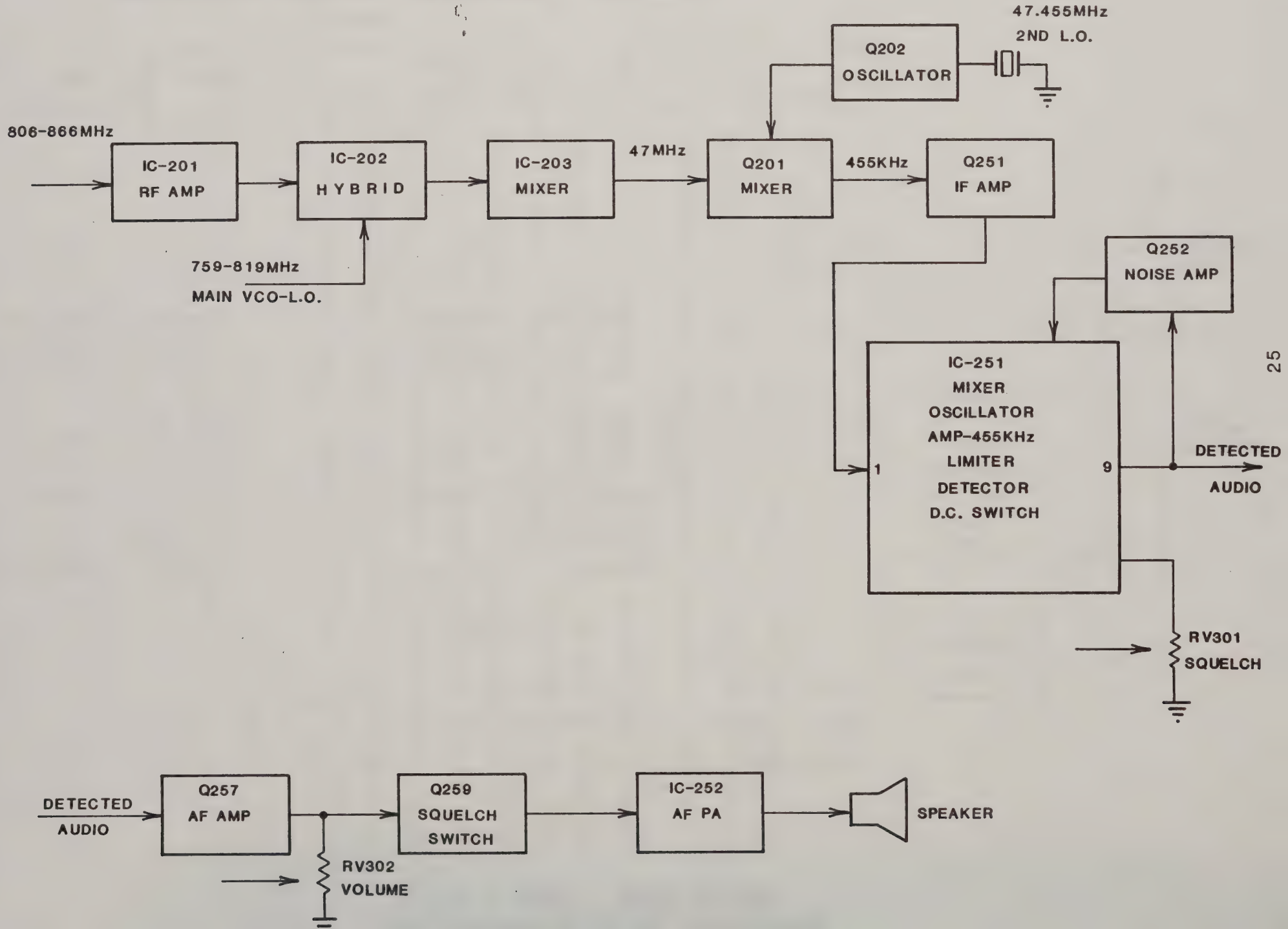
(1) UHF BAND

A: 406-430 MHz
B: 450-470 MHz
C: 470-494 MHz
D: 494-512 MHz
E: 430-450 MHz

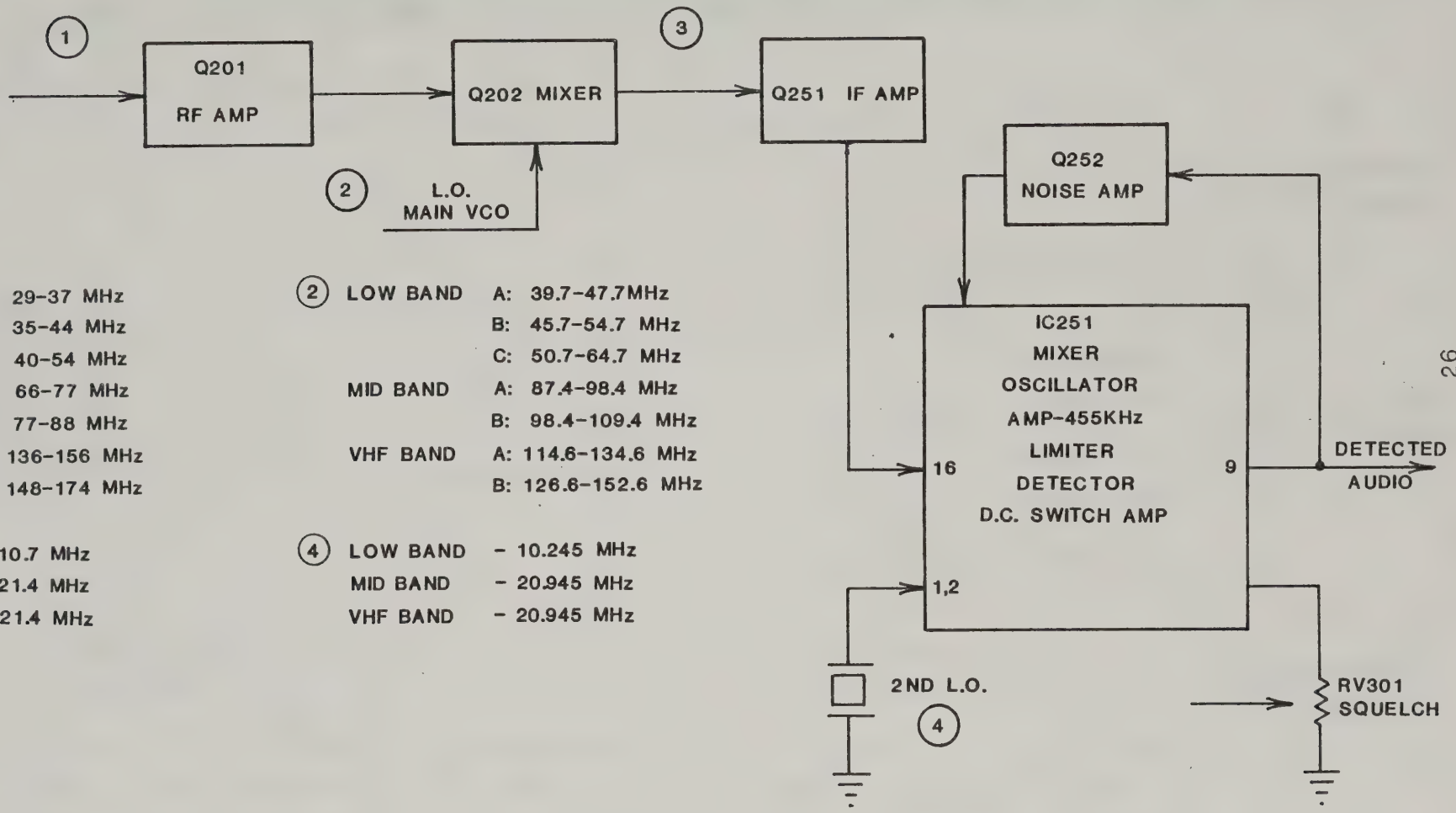
(2) UHF BAND

A: 384.6-408.6 MHz
B: 428.6-448.6 MHz
C: 448.6-472.6 MHz
D: 472.6-490.6 MHz
E: 408.6-428.6 MHz

RECEIVER BLOCK DIAGRAM - 800MHz



RECEIVER BLOCK DIAGRAM
LOW - MID - VHF BAND



(1) LOW BAND A: 29-37 MHz
B: 35-44 MHz
C: 40-54 MHz
MID BAND A: 66-77 MHz
B: 77-88 MHz
VHF BAND A: 136-156 MHz
B: 148-174 MHz

(2) LOW BAND A: 39.7-47.7MHz
B: 45.7-54.7 MHz
C: 50.7-64.7 MHz
MID BAND A: 87.4-98.4 MHz
B: 98.4-109.4 MHz
VHF BAND A: 114.6-134.6 MHz
B: 126.6-152.6 MHz

(3) LOW BAND - 10.7 MHz
MID BAND - 21.4 MHz
VHF BAND - 21.4 MHz

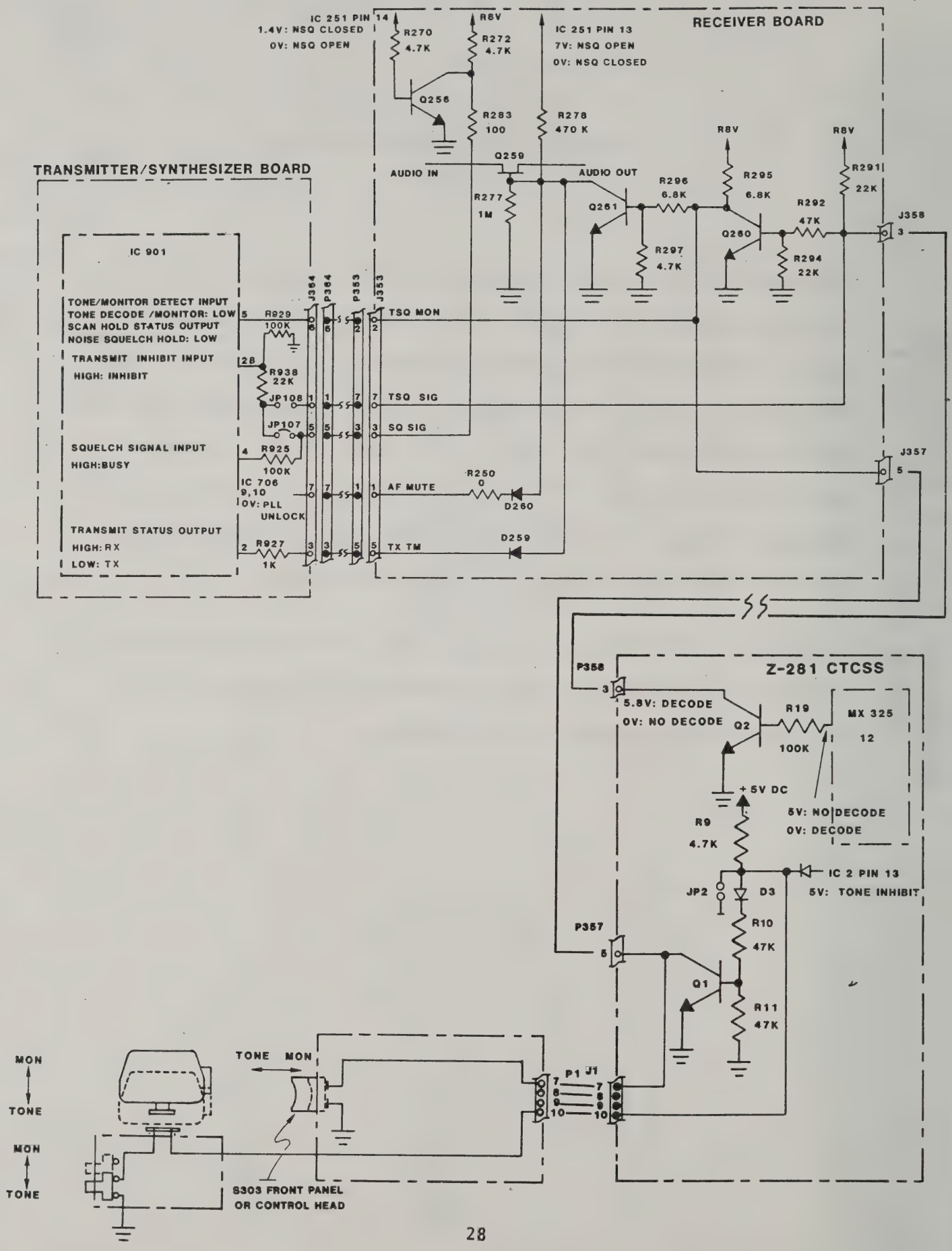
(4) LOW BAND - 10.245 MHz
MID BAND - 20.945 MHz
VHF BAND - 20.945 MHz

SQUELCH AND AUDIO AMPLIFIER

The noise from the detector is amplified by Q252, detected by D253 and controlled in level by the squelch control RV301. This detected noise signal is coupled to the DC switching amplifier of IC251. Under conditions of no RF signal, the detected noise signal increases and turns on the DC switching amplifier, which in turn biases off the transceiver audio squelch gate Q259. The detected audio signal is buffered by Q257 and passes through the volume control RV302 and squelch gate Q259 to the audio power amplifier IC252 and then to the speaker.

A simplified squelch circuit schematic is shown on the following page to enable the technician to break out the SYN-TECH squelch circuits for a better understanding of their operation.

SIMPLIFIED SQUELCH CIRCUIT SCHEMATIC



MICROCOMPUTER CHANNEL DATA TRANSFER

At unit power up a pulse is generated by Q405 resetting the microcomputer to an autotest mode. This reset pulse is applied to pin 15 on the microcomputer. A check is made to ensure the EPROM module is installed into the radio. If valed data is present at the EPROM, 3 bits of address data corresponding to the selected receive channel frequency are strobed from the microcomputer IC901 to the latch IC952. The remaining three bits of data are then strobed and latched in IC952. These 6 bits of data are transfered from the microcomputer IC901 pins 32 - 37. The EPROM data corresponding to the selected receive channel frequency is then strobed to the 8 bit shift register IC902 which transfers this data to the programmable divider IC701 under microcomputer control. This EPROM data is strobed to IC902 on pins 7, 6, 5, 4, 13, 14, 15, 1 and transferred to IC701 on pin 6. IC701 divides its input signal by the correct ratio to yield the desired receiver local oscillator frequency. The division ratio and receiver local oscillator frequencies for the different frequency ranges of radios is listed below.

MODEL	DIVISION RATIO		RECEIVER LOCAL OSC. FREQ.
Low Band	32/33	A Band	39.7 - 47.7 MHz
		B Band	45.7 - 54.7 MHz
		C Band	50.7 - 64.7 MHz
Mid Band	32/33	A Band	87.4 - 98.4 MHz
		B Band	98.4 - 109.4 MHz
VHF Band	64/65	A Band	114.6 - 134.6 MHz
		B Band	126.6 - 152.6 MHz
UHF BAnd	64/65	A Band	384.6 - 408.6 MHz
		B Band	428.6 - 448.6 MHz
		C Band	448.6 - 472.6 MHz
		D Band	472.6 - 490.6 MHz
		E Band	408.6 - 428.6 MHz
800 MHz	64/65		759.0 - 819.0 MHz

IC701 outputs on pin 10 an out-of-look signal, which is applied to pin 6 on the microcomputer IC901. This out-of-look signal mutes the receiver until phase lock is achieved. The microcomputer IC901 strobes data corresponding to the selected channel from pins 22-25 to the latched LED display drivers IC301 and IC302 on pins 7, 2, 1 and 6. IC301/302 in turn drive the channel LEDS. Brightness of the display is automatically adjusted to ambient light conditions by photosensor CDS301 and transistors Q301 and Q302.

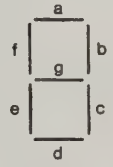
DRIVER'S & DISPLAY

OUTPUT IC901 PINS: 10,11			OUTPUT FROM IC901 PINS: 25,24,23,22				OUTPUT IC301 & 302 TO LED DISPLAY							
IC301,302 INPUT PINS =	5	4	3	6	2	1	7	13	12	11	10	9	15	14	
	ST			D	C	B	A	a	b	c	d	e	f	g	DISPLAY
	X	X	0	X	X	X	X	1	1	1	1	1	1	1	8
	X	0	1	X	X	X	X	0	0	0	0	0	0	0	BLANK
	0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
	0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
	0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
	0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
	0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
	0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
	0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
	0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
	0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
	0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
	0	1	1	1	0	1	0	0	0	0	0	0	0	0	BLANK
	0	1	1	1	0	1	1	0	0	0	0	0	0	0	"
	0	1	1	1	1	0	0	0	0	0	0	0	0	0	"
	0	1	1	1	1	0	1	0	0	0	0	0	0	0	"
	0	1	1	1	1	1	0	0	0	0	0	0	0	0	"
	0	1	1	1	1	1	1	0	0	0	0	0	0	0	"
	1	1	1	X	X	X	X								*

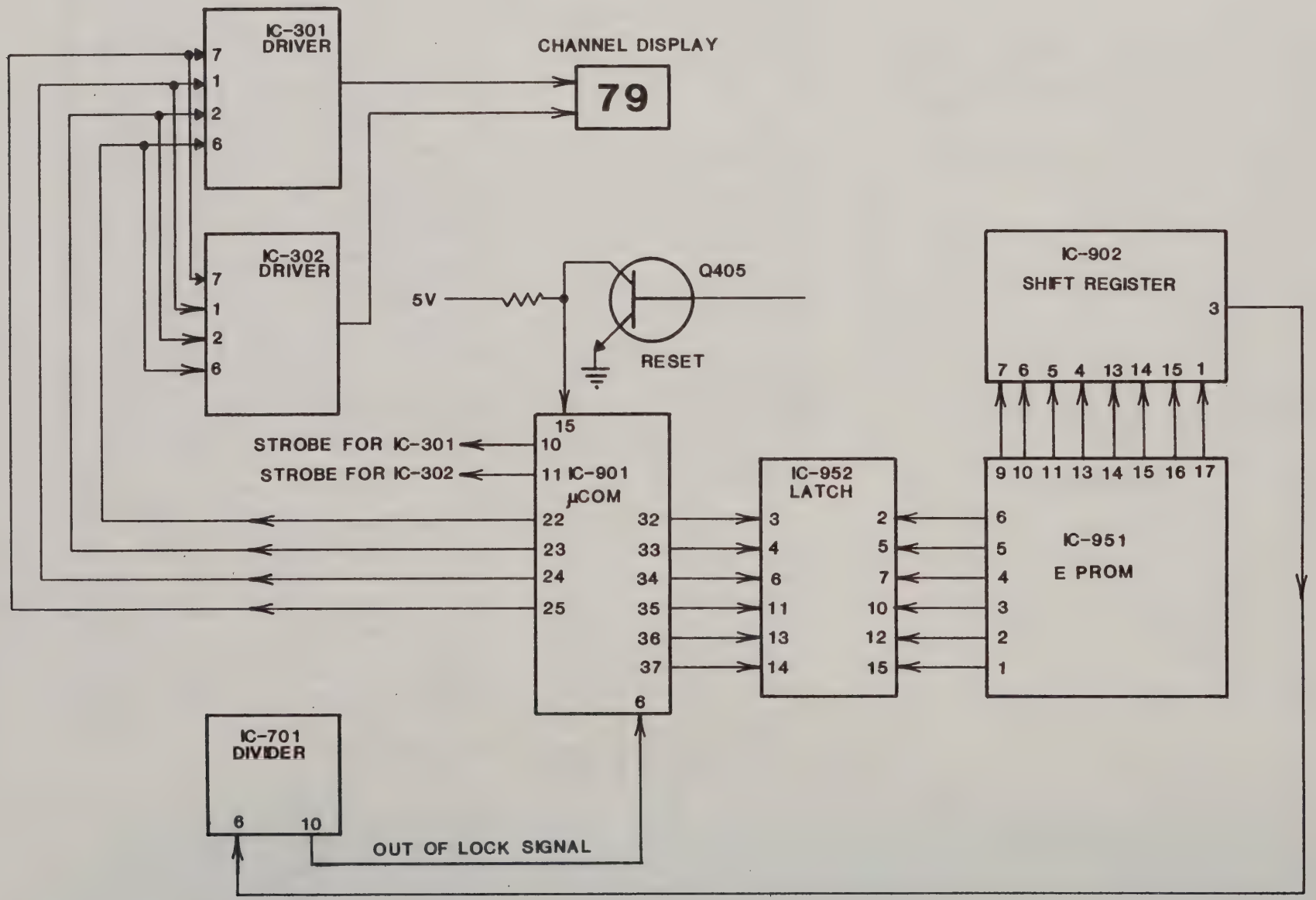
(0 = 0 TO 2V) (1 = 6 TO 8V)

X = DON'T CARE

* = DEPENDS UPON BCD CODE PREVIOUSLY APPLIED WHEN ST = 0



MICRO COMPUTER CHANNEL DATA TRANSFER BLOCK DIAGRAM

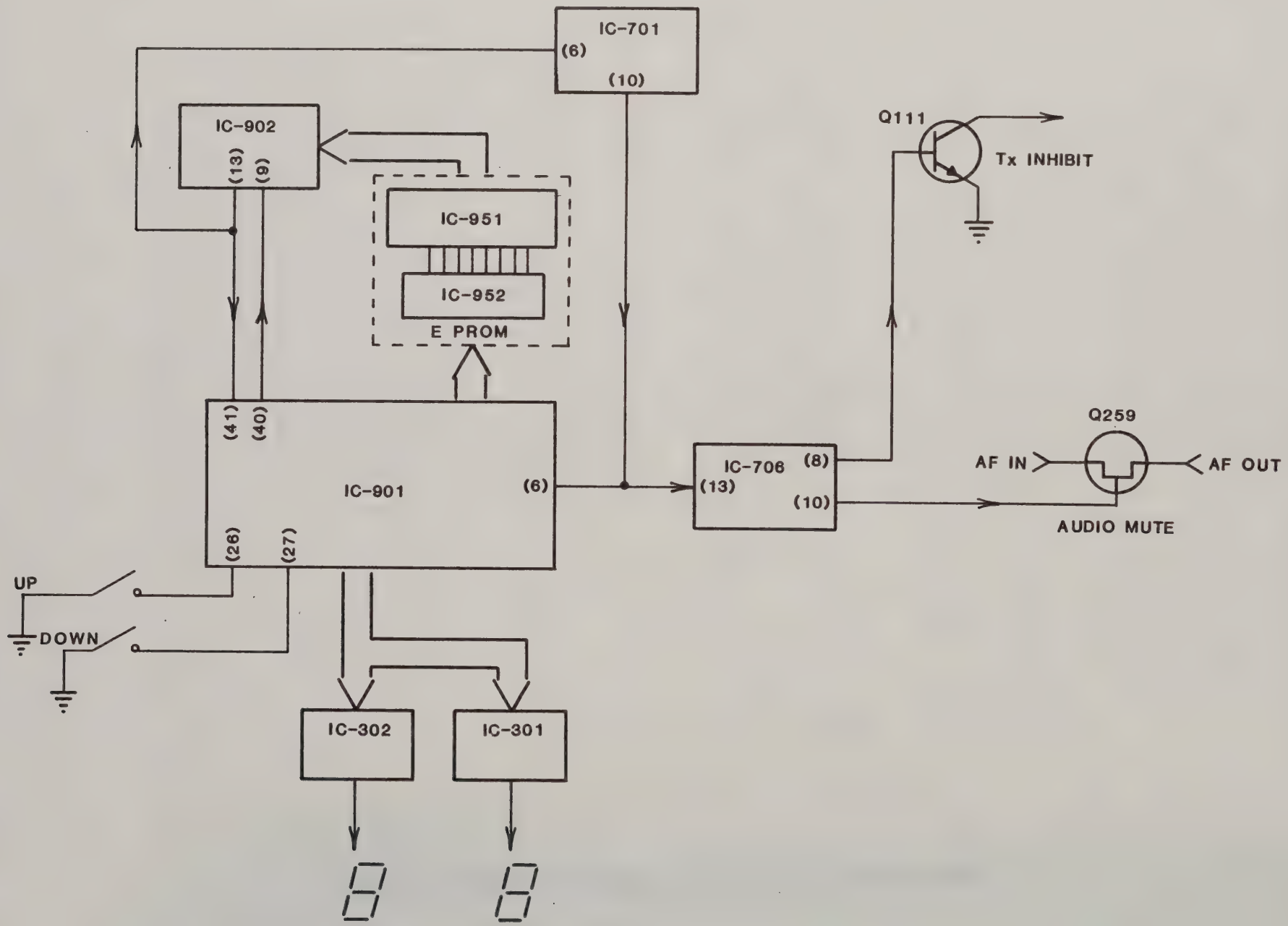


MANUAL CHANNEL SELECTION

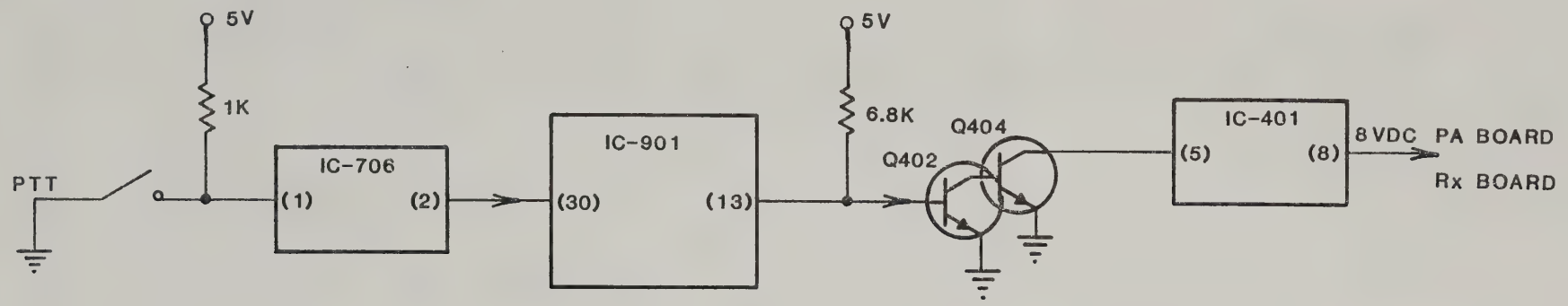
Activation of the up-down channel selector switch is sensed by the microcomputer on pins 26 and 27. If the channel selector switch is moved to the up position, pin 26 goes low. If the channel selector switch is moved to the down position, pin 27 will go low. The receive audio is muted when ever the channel selector switch is moved up or down. Upon release of the channel selector switch, EPROM data corresponding to the new channel is strobed to the programmable divider IC701 on pin 6. If the synthesizer lock signal is not detected after a channel change, (indicated by a lack of a logic low on pin 10 of IC701), the receiver and transmitter are inhibited and the channel indicator displays an error code 95. The receiver/transmitter inhibit signal is a logic low which comes from the microcomputer IC901 pin 6. The low from IC901 pin 6 will be inverted to a high by the invert gate IC706. This logic high is used to turn on Q111, which will prevent any transmitted signal from reaching the power amplifier. The logic low from IC901 pin 6 is also transfered to the receiver board via J364 pin 7 on the transmit board in order to mute the receiver during th 95 error code condition.

When the PTT is depressed, a logic low is applied to the inverter gate IC706. This logic low is inverted into a logic high and applied to the Microcomputer PTT input pin 30. The microcomputer outputs this PTT signal as a logic low on pin 13. This low from IC901 pin 13 is routed to pin 5 of IC401, the 8VDC regulator. When pin 5 is pulled low, pin 6, the receive 8 volt line is inhibited and pin 8, the transmit 8 volt line outputs 8VDC. The microcomputer then outputs EPROM address data corresponding to the selected transmit channel, which results in the programmable divider IC701 being reprogrammed for the correct transmit frequency. The chain of events which will take place have been discussed under the heading MODULATOR AND TRANSMIT PLL.

MANUAL CHANNEL SELECTION
BLOCK DIAGRAM



PTT FLOW CHART BLOCK DIAGRAM



SCAN OPERATION

When scan operation is selected by activation of either of the push buttons on the radio front panel, pin 9 (PRI) or pin 8 (SCN) on the microcomputer IC901 is pulled low. The transmit and receive addresses of the displayed channel are stored in microcomputer memory as the priority channel. The displayed channel information is sent from IC301 and IC302 pins 7, 1, 2 and 6 and transmitted to the microcomputer on pins 22, 23, 24 and 25. The address data corresponding to the first scan channel is strobed to the latch IC952 directly from the EPROM, resulting in the generation of the correct local oscillator frequency as described in the section titled REFERENCE OSCILLATOR AND MAIN PLL. After synthesized lock is achieved, a 25 millisecond period (Interval A) is alloted for operation of the noise squelch circuitry. At the end of Interval A, one of four sequences of events will take place as described below.

1) The microcomputer causes the scan sequence to resume (noise squelch closed). The microcomputer senses the closed squelch condition from a signal transmitted from IC251 on the receiver board. If the squelch is closed, pin 14 of IC251 will be at 1.4 volts. This will turn on transistor Q255 causing the high to be inverted to a low. This logic low will be transmitted to the microcomputer IC901 pin 4 which is labeled SQSIG.

2) The microcomputer opens the audio squelch gate (noise squelch open and the noise squelch mode is programmed into the EPROM or the CTCSS mode is programmed into the EPROM and no CTCSS tone is programmed on the specific receive channel). IC901, pin 5, labeled TSQMON goes logic low and transmits this signal to Q261 (squelch switch) which turns it off. With Q261 turned off, Q259 turns on and allows the receive audio to pass.

3) The microcomputer activates the Interval B timer (noise squelch open and the CTCSS scan mode is programmed into the EPROM and CTCSS is programmed on the specific receive channel). Interval B is a time period alloted for signaling system decoder operation. The time period is 300 milliseconds. At the end of Interval B, one of two sequenses of events will take place as described below.

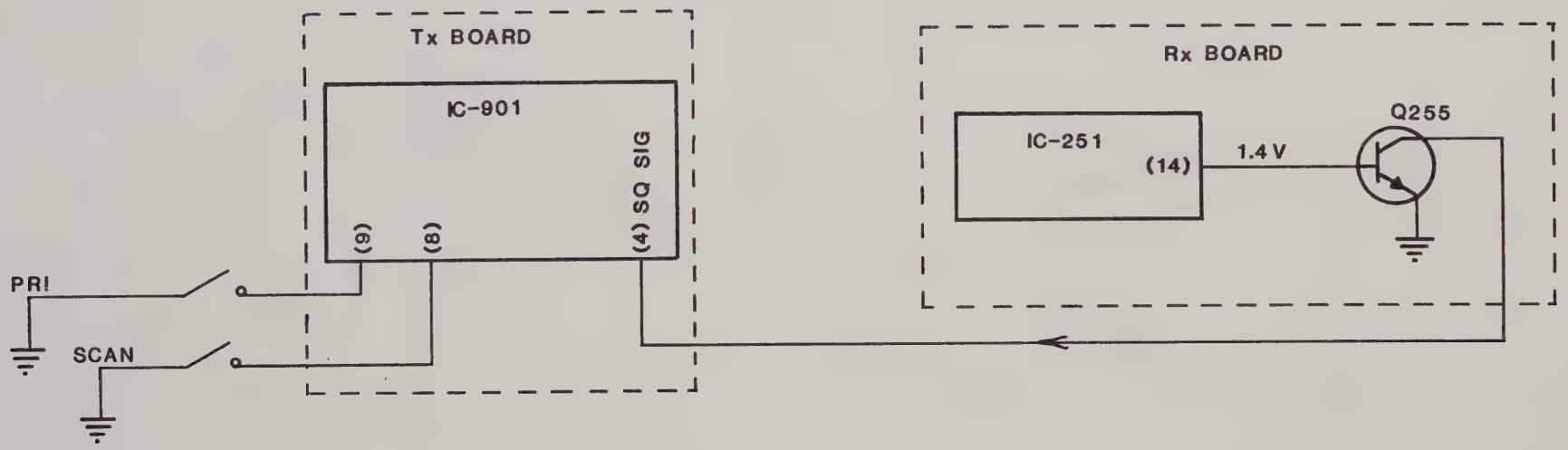
   A) The microcomputer causes the scanning sequence to resume because of no decoder output, indicated by a high level on the TSQMON line at IC901 pin 5. The collector of Q2 on the CTCSS board is held at 0 volts, which will turn off Q260 on the receiver board causing its collector to go high. This high is transmitted to IC901, pin 5.

   B) The microcomputer causes the audio squelch to open because of a successful decode output indicated by

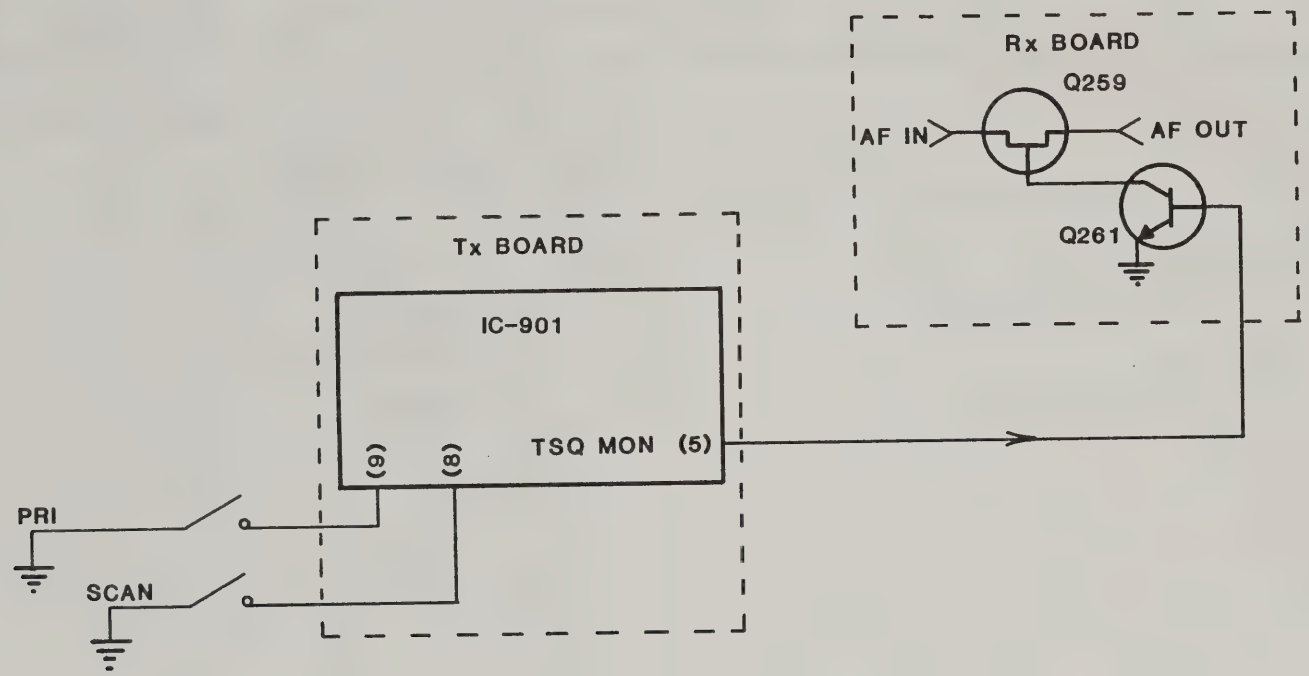
a low input to IC901, pin 5. If successful decode is achieved, the collector of Q2 on the CTCSS board will go high, which will turn Q260 on the receiver board to the on state. The collector of Q260 will be pulled low when Q260 is turned on and this low will be transmitted to IC901, pin 5.

If the receive channel corresponds to the operated selected priority channel, a two-beep signal is generated when the squelch gate opens. After squelch closure, scan resumption is delayed by the amount of the programmable delay timer (RX or TX). If the priority-sampling scan mode is selected, the microcomputer automatically checks the priority channel after every fourth or eighth non-priority channel (programmable). While in a hold condition on a non-priority channel, the priority channel is sampled every second or two seconds (programmable). The priority channel sampling sequence is identical to the normal scan procedure described above.

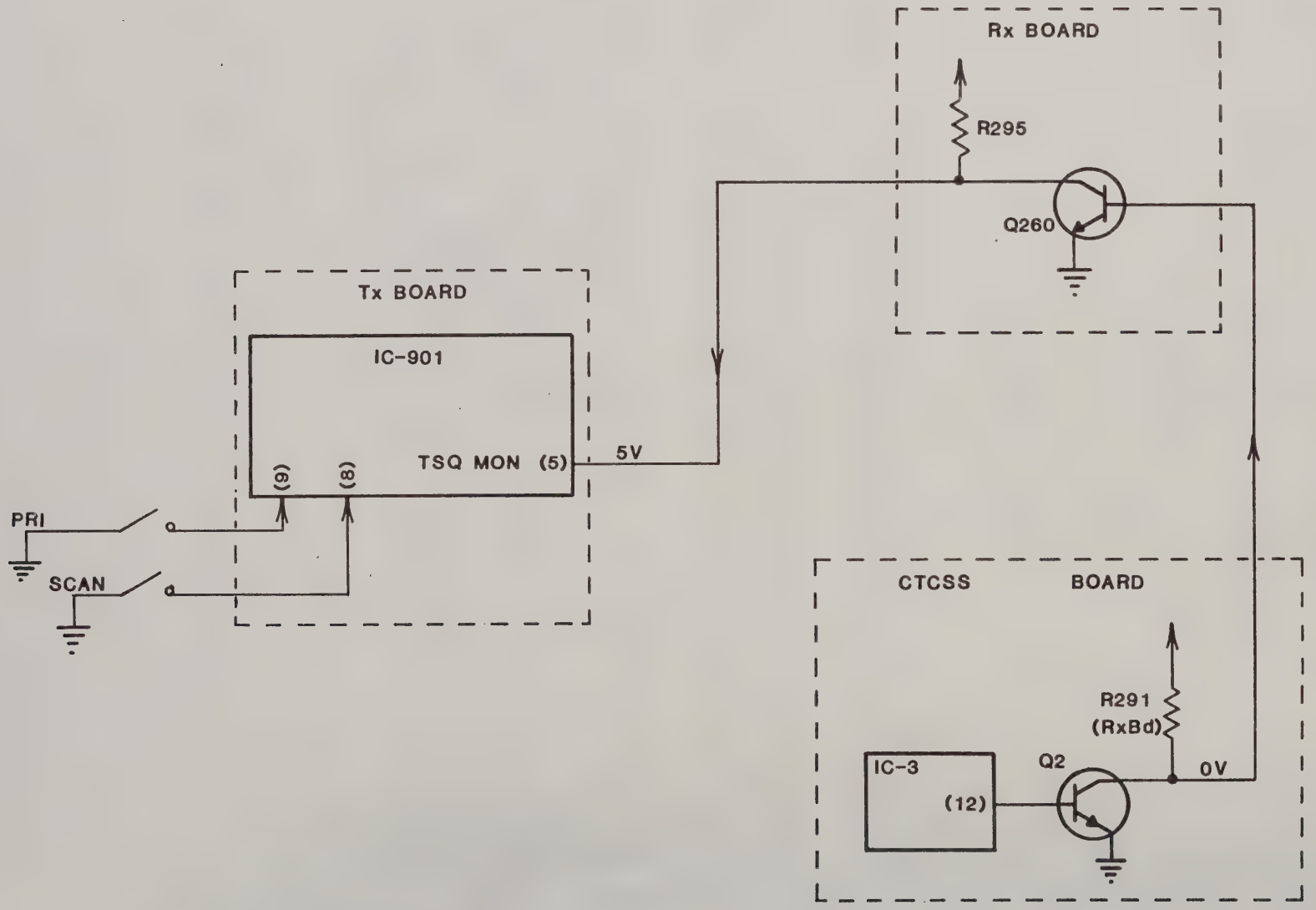
SCAN BLOCK DIAGRAM NOISE SQUELCH CLOSED (RESUME SCAN)



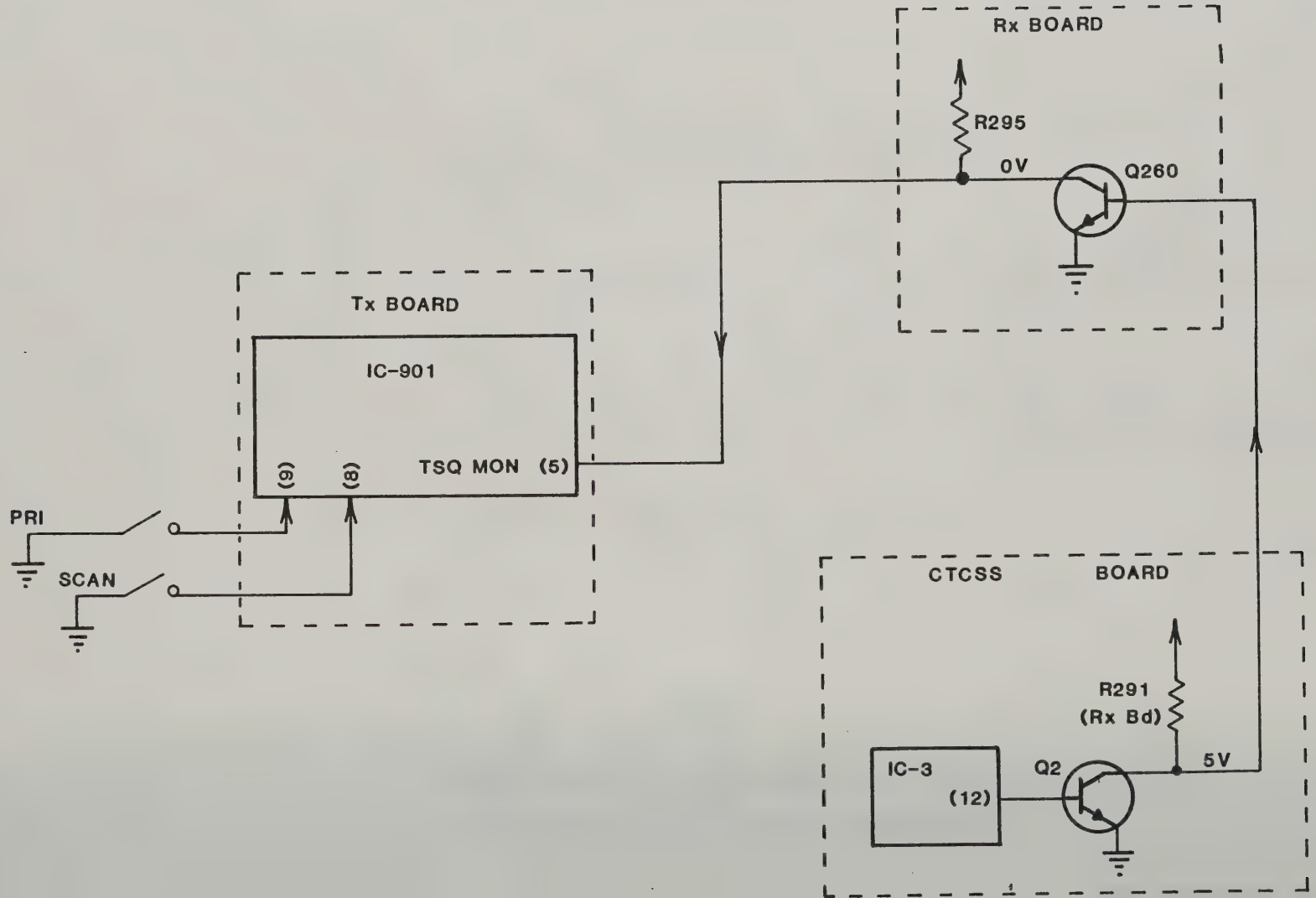
SCAN BLOCK DIAGRAM
NOISE SQUELCH OPEN (SCAN STOP)



SCAN BLOCK DIAGRAM
TONE SQUELCH (RESUME SCAN)



SCAN BLOCK DIAGRAM
TONE SQUELCH (SCAN STOP)



BUSY CHANNEL LOCKOUT AND TIME OUT TIMER

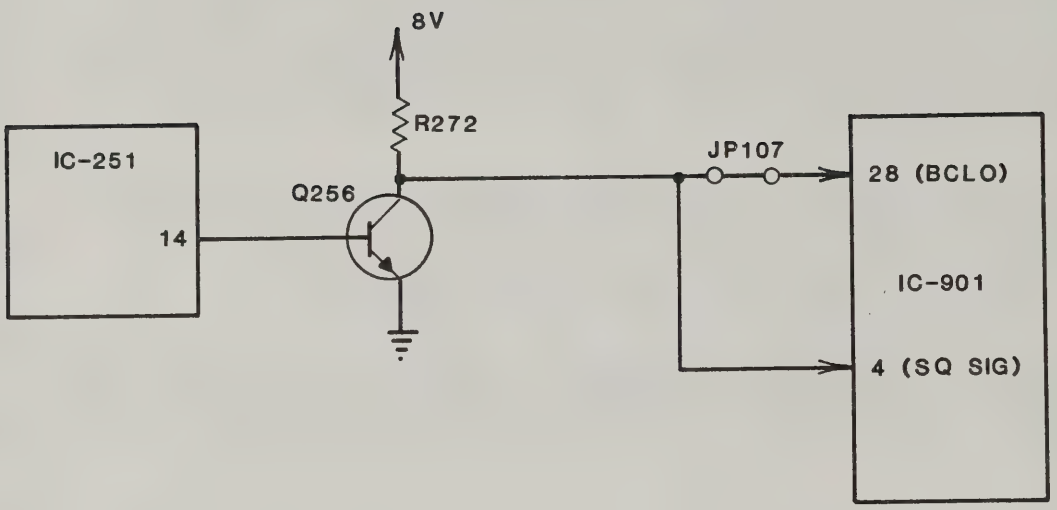
The busy channel lockout function can be jumper selected by JP107 or JP108 to provide transmitter inhibit on either carrier or CTCSS/CDCSS tone. If the busy channel signal is carrier only, pin 14 of IC251 on the receiver board will be at 0 volts. This logic low is transfered to the base of Q256 (squelch switch) which causes it to turn off. With Q256 turned off, the collector of Q256 is held high through R272 which transfers this high to the microcomputer IC901 pin 28 (PTT inhibit). If the busy channel signal is composed of carrier and tone, the collector of Q2 on the CTCSS board is held high through R291 on the receiver board. This high is transfered to the microcomputer IC901 pin 28 (PTT inhibit).

If the Busy Channel Lockout function is programmed in the EPROM, transmit will be inhibited while the busy channel signal is present. An audio alert signal (if programmed) is generated when the transmitter is keyed to indicate the channel busy condition.

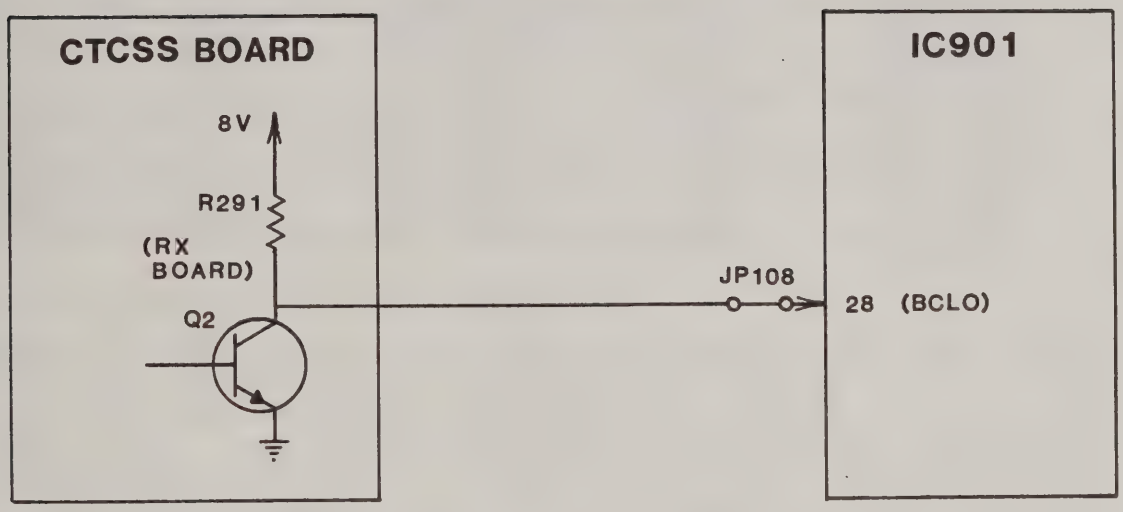
The Time OUT Timer function is completely internal to the microcomputer. If the continuous transmit time exceeds the time limit programmed into the EPROM, the transmitter is disabled and an audio beep alerts the operator.

BUSY CHANNEL LOCKOUT BLOCK DIAGRAM

CARRIER SQUELCH



BUSY CHANNEL LOCKOUT BLOCK DIAGRAM
TONE SQUELCH



The CTCSS option provides, under microcomputer control, encode and decode of 35 standard EIA CTCSS tones. At each channel change and transmit/receive transition, data corresponding to the selected channel and mode is strobed from J903 on the EPROM to P903 on the CTCSS board. The data is strobed on lines D0 to D4 and follows the logic pattern listed in the table below for the different CTCSS tones.

ENCODE/DECODE FREQUENCY (HZ)	IC 3 PINS 4	5	6	7	8	9
67.0	1	1	1	1	1	1
71.9	0	1	1	1	1	1
74.4	1	1	1	1	1	0
77.0	0	0	1	1	1	1
79.7	1	1	1	1	0	1
82.5	0	1	1	1	1	0
85.4	1	1	1	1	0	0
88.5	0	0	1	1	1	0
91.5	1	1	1	0	1	1
94.8	0	1	1	1	0	1
97.4	1	1	1	0	1	0
100.0	0	0	1	1	0	1
103.5	0	1	1	1	0	0
107.2	0	0	1	1	0	0

ENCODE/DECODE FREQUENCY (HZ)	IC 3 PINS 4	5	6	7	8	9
110.9	0	1	1	0	1	1
114.8	0	0	1	0	1	1
118.8	0	1	1	0	1	0
123.0	0	0	1	0	1	0
127.3	0	1	1	0	0	1
131.8	0	0	1	0	0	1
136.5	0	1	1	0	0	0
141.3	0	0	1	0	0	0
146.2	0	1	0	1	1	1
151.4	0	0	0	1	1	1
156.7	0	1	0	1	1	0
162.2	0	0	0	1	1	0

ENCODE/DECODE FREQUENCY (HZ)	IC 3 PINS 4	5	6	7	8	9
167.9	0	1	0	1	0	1
173.8	0	0	0	1	0	1
179.9	0	1	0	1	0	0
186.2	0	0	0	1	0	0
192.8	0	1	0	0	1	1
203.5	0	0	0	0	1	1
210.7	0	1	0	0	1	0
218.1	0	0	0	0	0	0
225.7	0	1	0	0	0	1
233.6	0	0	0	0	0	1
241.8	0	1	0	0	0	0
250.3	0	0	0	0	0	0

The D0 to D4 data is latched into IC1 on the CTCSS board. IC1 outputs this data to IC3 for generation or detection of the correct CTCSS tone. This data is also input to IC2, which outputs a high logic level for encode/decode inhibit if all data lines D0 to D4 are low. All data lines would be low if no CTCSS tone is desired on a specific channel and an AUX code "0" is programmed on that channel. Encode inhibit is accomplished by holding IC3 pin 17 at a high level through D2, which is biased high through IC2 pin 13 since all inputs to IC2 would be low. Decode is inhibited by biasing Q1 on through D4, which is biased high through IC2 pin 13 since all inputs to IC2 would be low. With Q1 turned on, its collector is pulled low. As long as the collector of Q1 is pulled low, the base of Q261 on the receiver board is also held low. The collector of Q261, which is also connected to the gate of the squelch FET, is then under control of the noise squelch signal from IC251 pin 13. If the squelch is open, pin 13 will be high. If the squelch is closed, pin 13 will be low. If the gate of the squelch FET (Q259) is held high, audio will pass. If the gate of the squelch FET is held low, no audio will pass.

If decode is not inhibited by Aux Code 0 programming, control of the squelch FET is by IC251 pin 13 and Q261. Q261 is controlled by Q260, which in turn is controlled by Q2 on the CTCSS board. Q2 is normally biased on by IC3 pin 12 which outputs a logic low to the base of Q260 on the receiver board. The collector of Q260 will be pulled high through R295 and transfer this high to the microcomputer pin 5 (TSQMON). Q2 on the CTCSS board is switched off when the correct tone is detected and its collector is pulled high by R291 on the receiver board. This high will turn on Q260 which will pull the collector of Q260 low. This low will be tranferred to pin 5 on the microcomputer (TSQ MON).

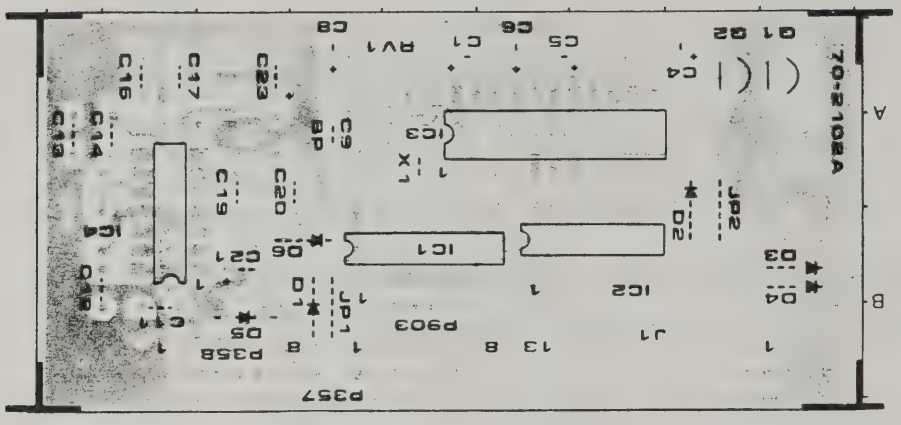
CTCSS OPERATION

The monitor switch and hang up box both control the status of Q1 on the CTCSS board and thus allow or inhibit squelch gate control by the CTCSS board in the same manner as Aux Code "0" programming.

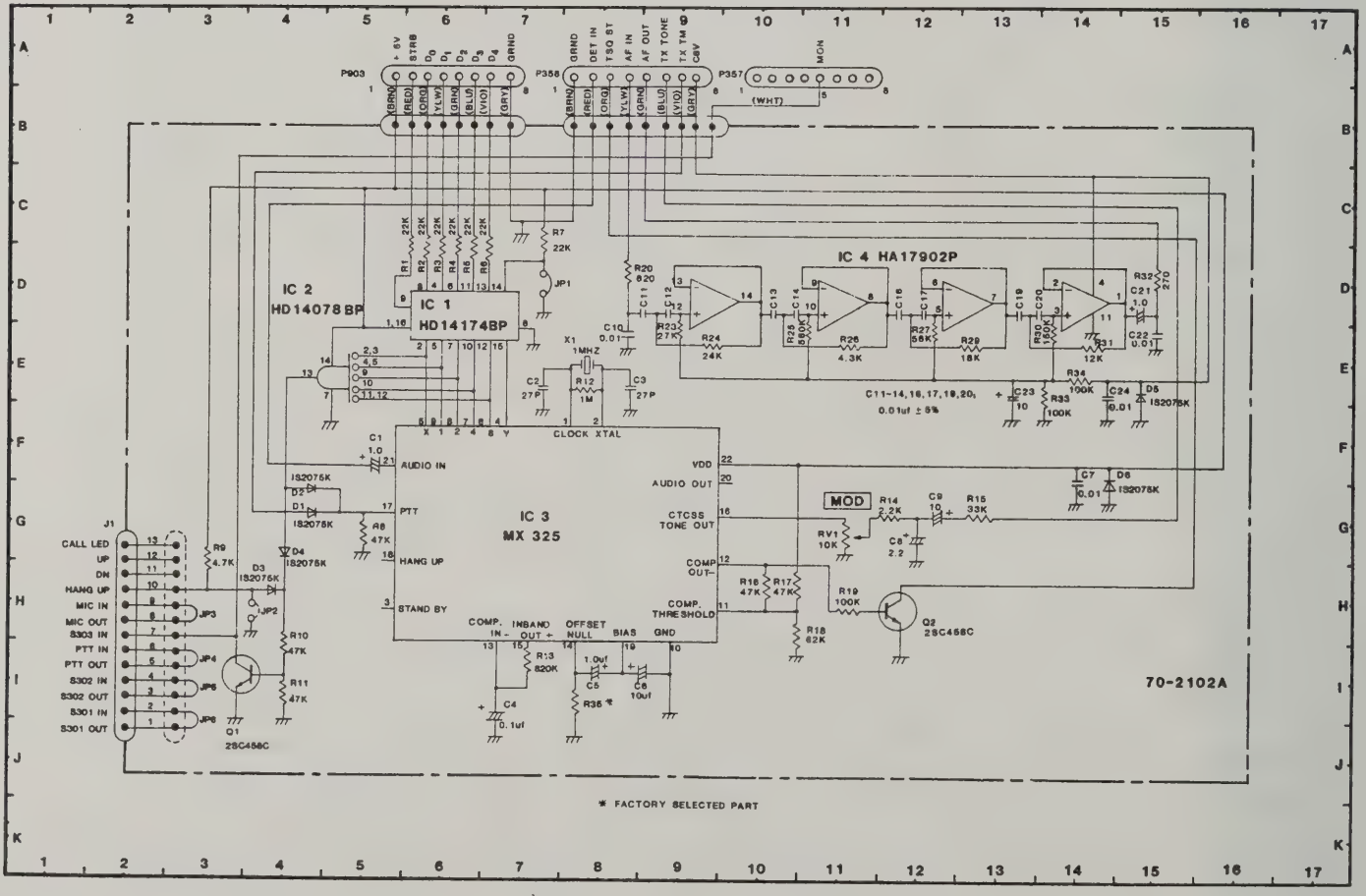
Crystal X1 generates a stable reference for IC3 tone generation and detection. IC4 functions as an audio highpass filter to remove CTCSS tones from the speaker audio. Encode tone output is from IC3 pin 16 with tone modulation level adjustable by RV1.

70-2102A CTCSS PC BOARD AND SCHEMATIC

CTCSS PCB (TOP VIEW)

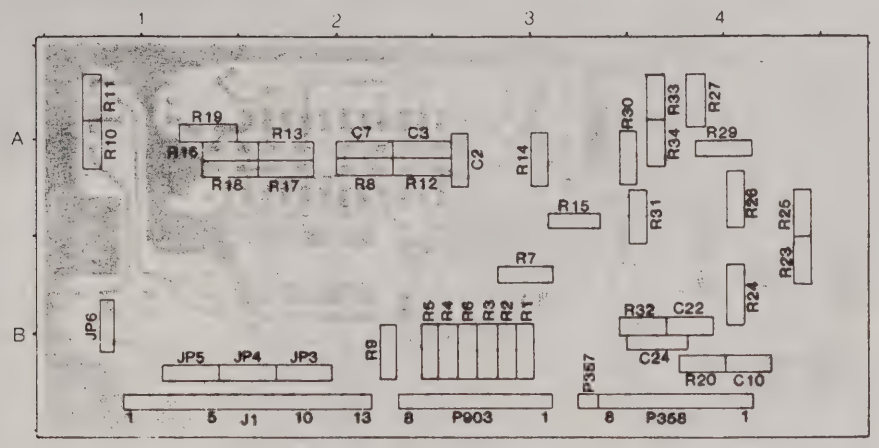


CTCSS SCHEMATIC DIAGRAM



70-2102A CTCSS PC BOARD

CTCSS PCB (BOTTOM VIEW)



CTCSS VOLTAGE CHARTS

TRANSISTORS

REF. NO.	DESCRIPTION		BASE	COLLECTOR	EMITTER	FUNCTION
Q1	2SC458C					Squelch Control
	W/Tone	Mon. ON	0.0	0.0	0.0	
		Mon. OFF	0.0	.050	0.0	
		W/"0" Code	.650	.050	0.0	
	W/O Tone	Mon. ON	0.0	0.0	0.0	
		Mon. OFF	0.0	4.44	0.0	
Q2	2SC458C					Tone Squelch Switch
		Decode	0.0	5.85	0.0	
		No Decode	.639	0.0	0.0	

INTEGRATED CIRCUITS

REF. NO.	DESCRIPTION	PIN NO.	+ V VOLTAGE	GND. PIN NO.	FUNCTION
IC 1	HD14174BP	16	5V	8	Data Latch
IC 2	HD14078BP	14	5V	7	Encode/Decode Inhibiter
IC 3	MX 325	22	5V	10	Encoder/Decoder
IC 4	HA17902P	4	8V	11	High Pass Filter

ENCODE/DECODE FREQUENCY (HZ) — IC 3 PINS

	4	5	6	7	8	9
67.0	1	1	1	1	1	1
71.9	0	1	1	1	1	1
74.4	1	1	1	1	1	0
77.0	0	0	1	1	1	1
79.7	1	1	1	1	0	1
82.5	0	1	1	1	1	0
85.4	1	1	1	1	0	0
88.5	0	0	1	1	1	0
91.5	1	1	1	0	1	1
94.8	0	1	1	1	0	1
97.4	1	1	1	0	1	0
100.0	0	0	1	1	0	1
103.5	0	1	1	1	0	0
107.2	0	0	1	1	0	0

ENCODE/DECODE FREQUENCY (HZ) — IC 3 PINS

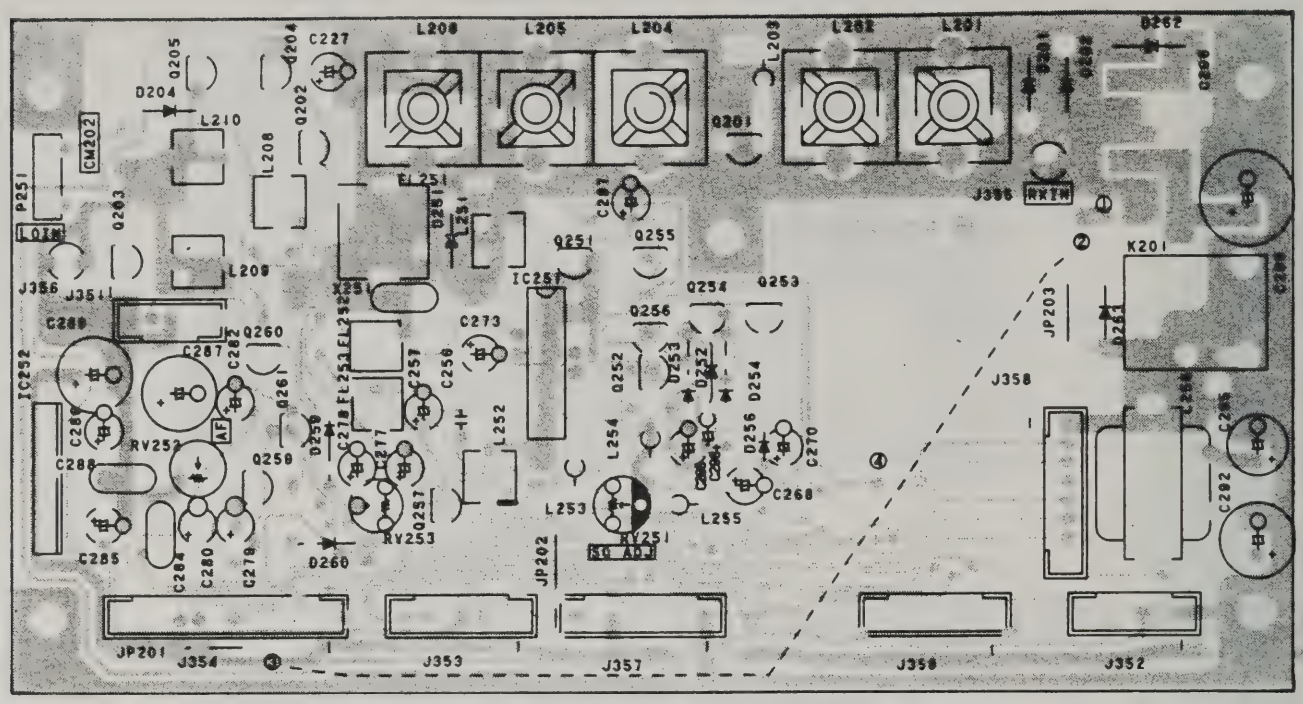
	4	5	6	7	8	9
110.9	0	1	1	0	1	1
114.8	0	0	1	0	1	1
118.8	0	1	1	0	1	0
123.0	0	0	1	0	1	0
127.3	0	1	1	0	0	1
131.8	0	0	1	0	0	1
136.5	0	1	1	0	0	0
141.3	0	0	1	0	0	0
146.2	0	1	0	1	1	1
151.4	0	0	0	1	1	1
156.7	0	1	0	1	1	0
162.2	0	0	0	1	1	0

ENCODE/DECODE FREQUENCY (HZ) — IC 3 PINS

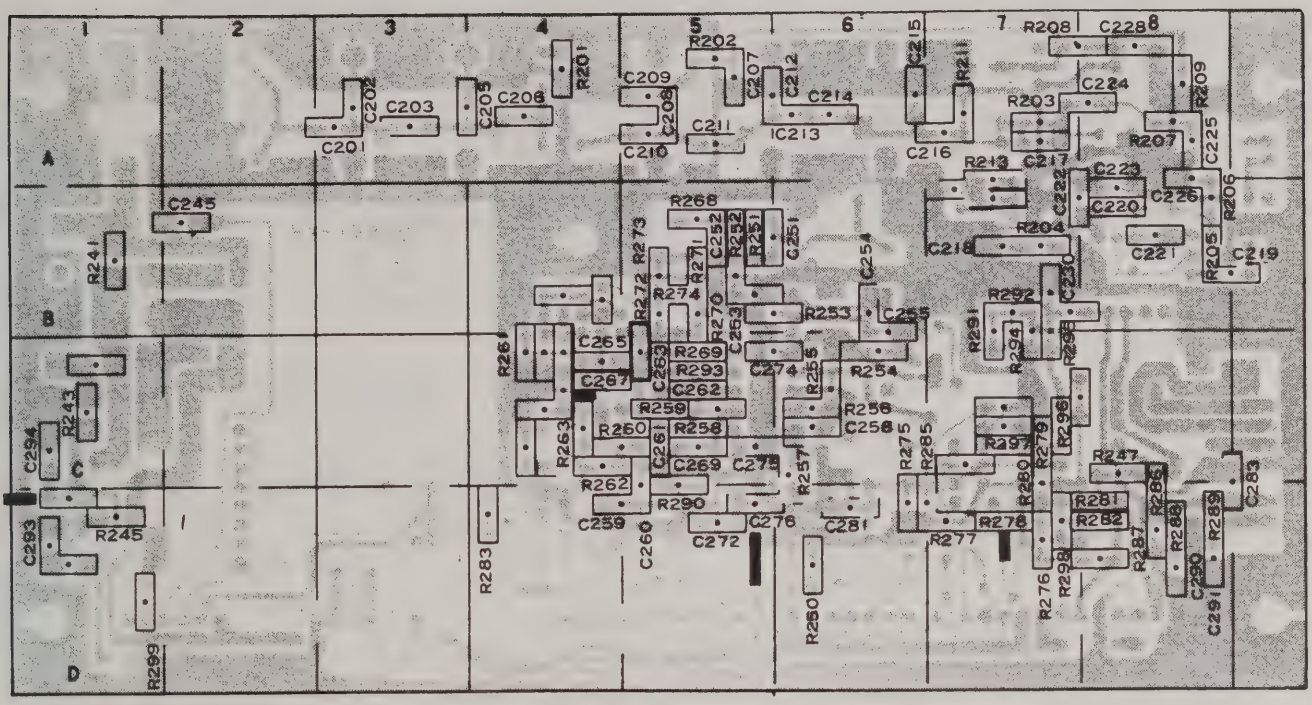
	4	5	6	7	8	9
167.9	0	1	0	1	0	1
173.8	0	0	0	1	0	1
179.9	0	1	0	1	0	0
186.2	0	0	0	1	0	0
192.8	0	1	0	0	1	1
203.5	0	0	0	0	1	1
210.7	0	1	0	0	1	0
218.1	0	0	0	0	0	0
225.7	0	1	0	0	0	1
233.6	0	0	0	0	0	1
241.8	0	1	0	0	0	0
250.3	0	0	0	0	0	0

"1" = 5V
"0" = 0V

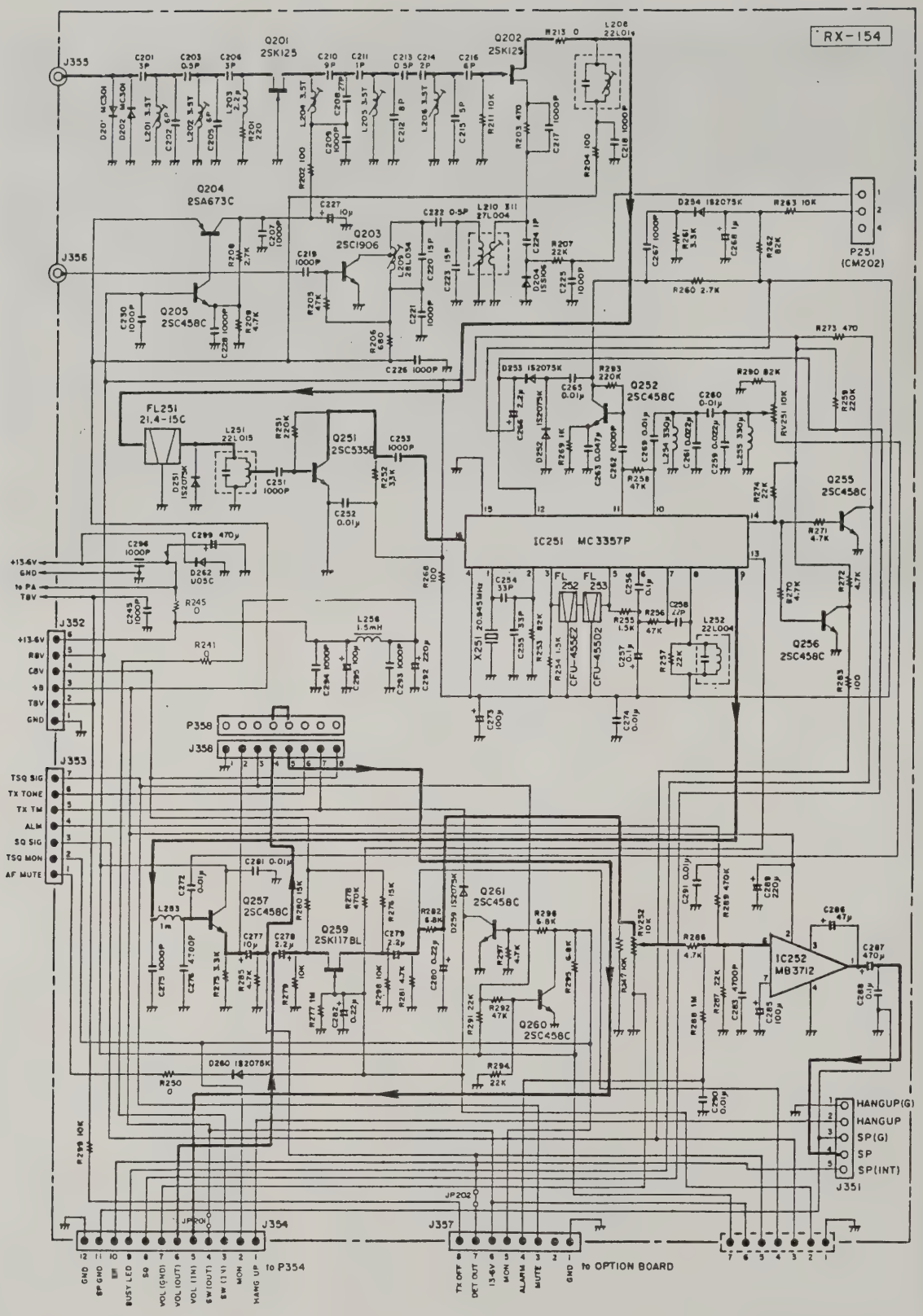
RECEIVER PC BOARD (TOP VIEW)



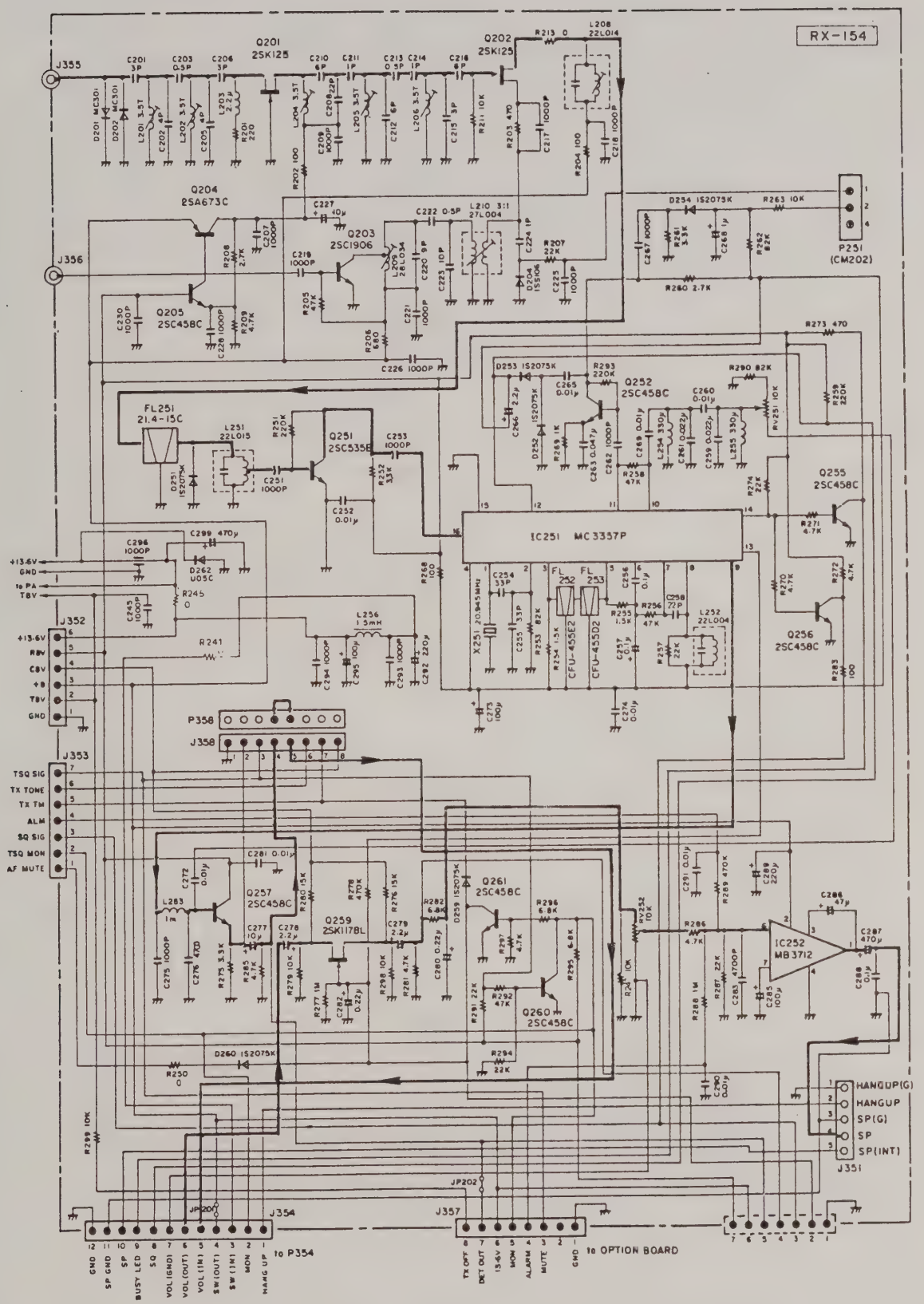
ECEIVER PC BOARD (BOTTOM VIEW)

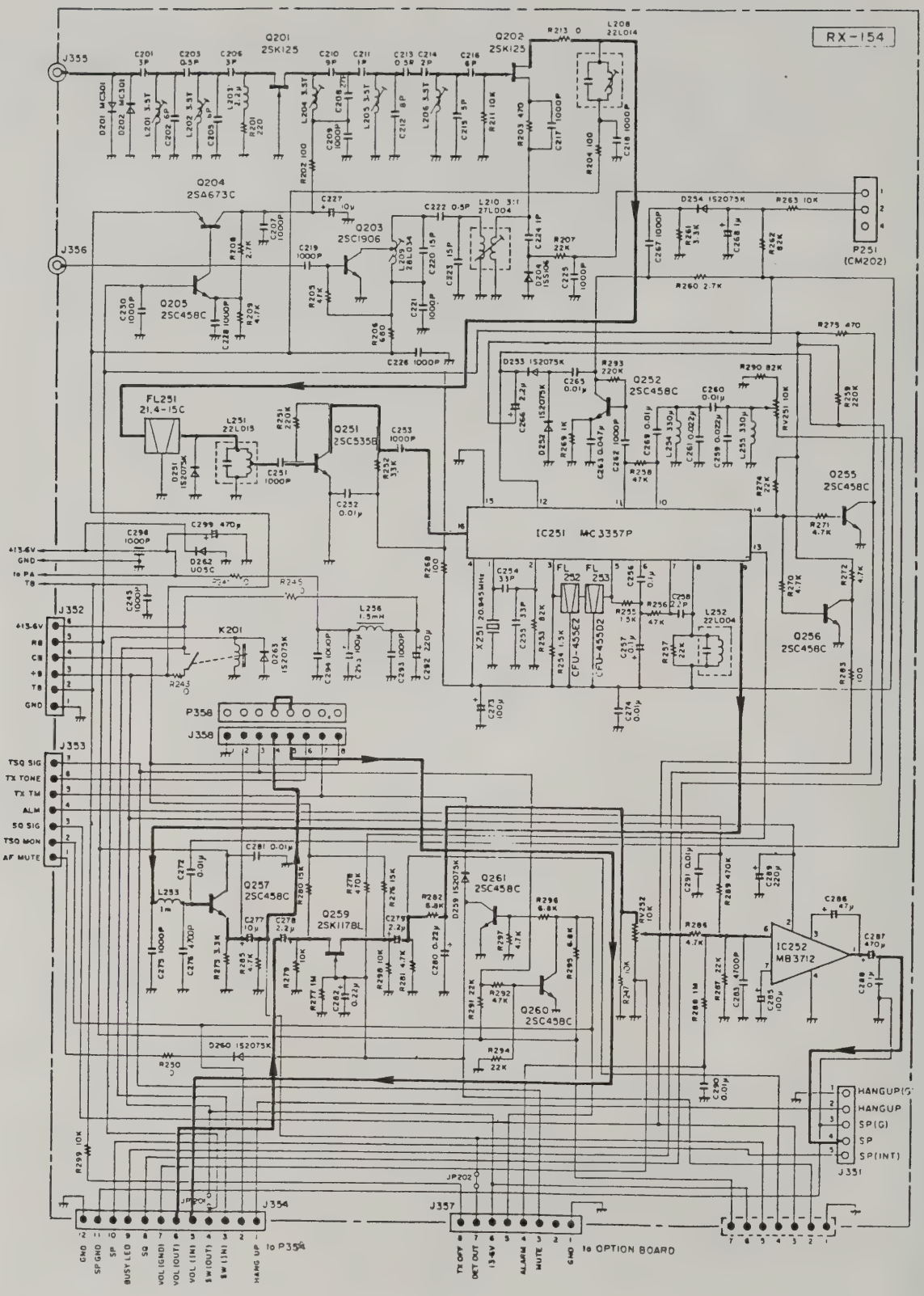


RECEIVER SCHEMATIC DIAGRAM

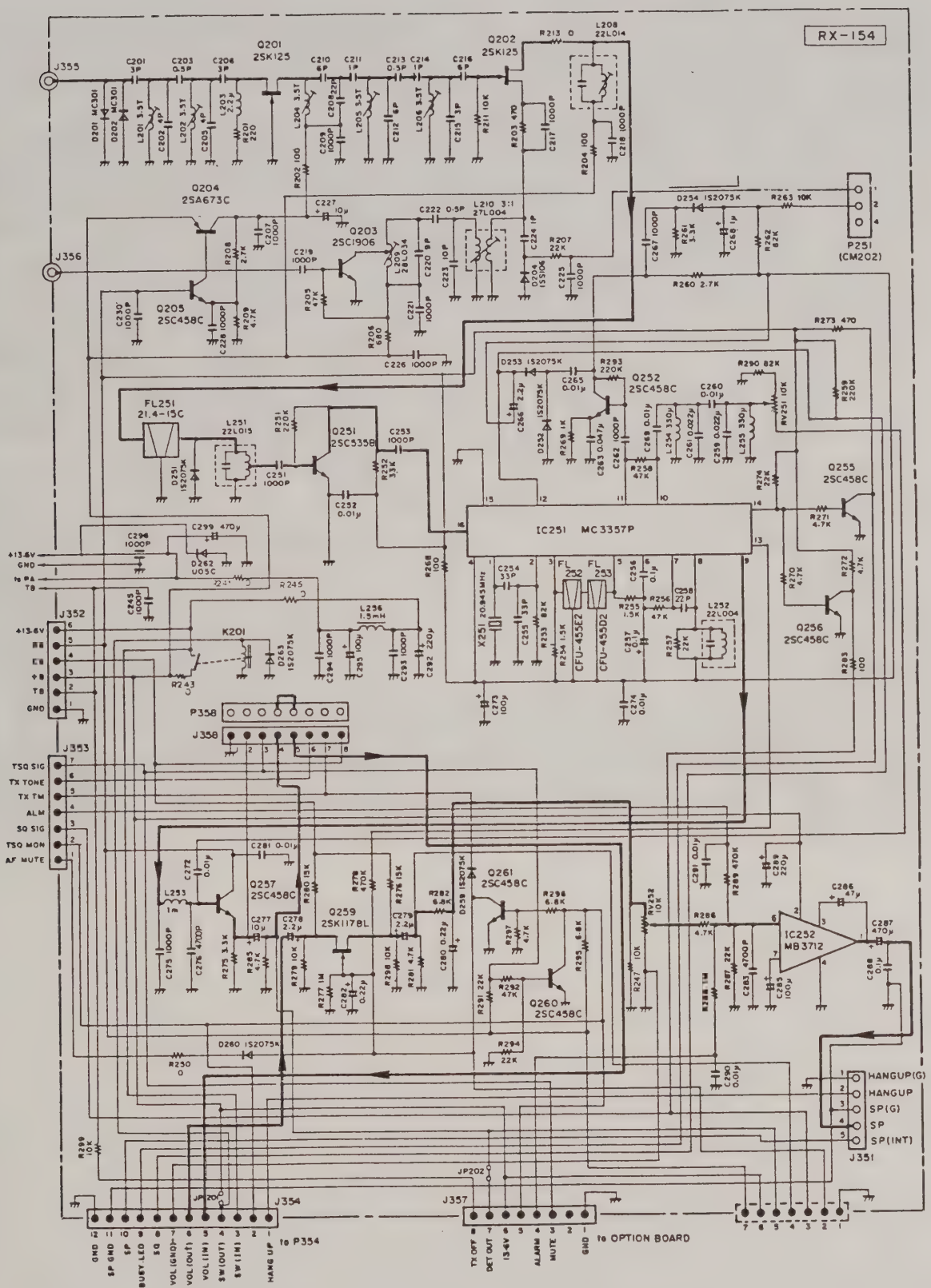


RECEIVER SCHEMATIC DIAGRAM

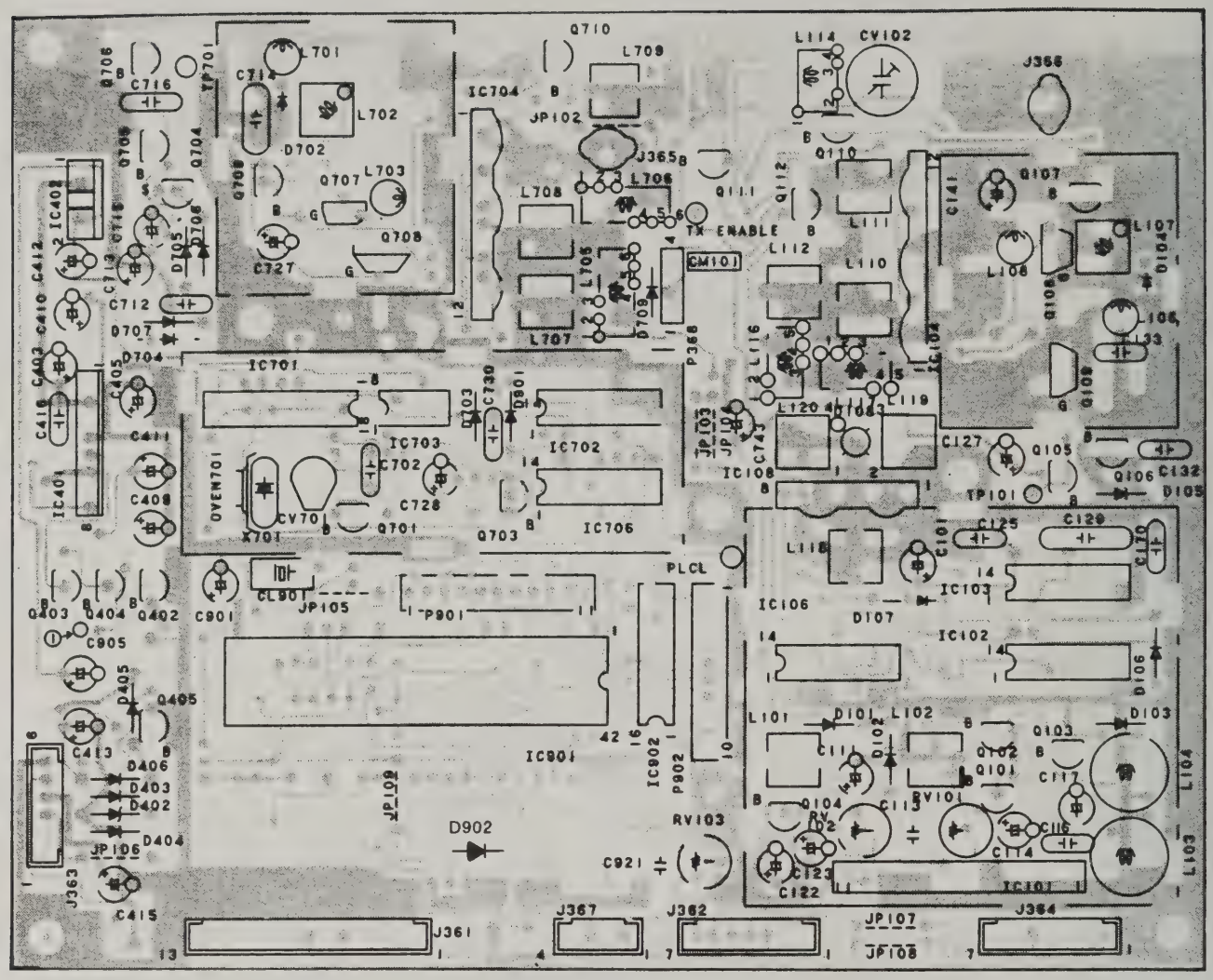


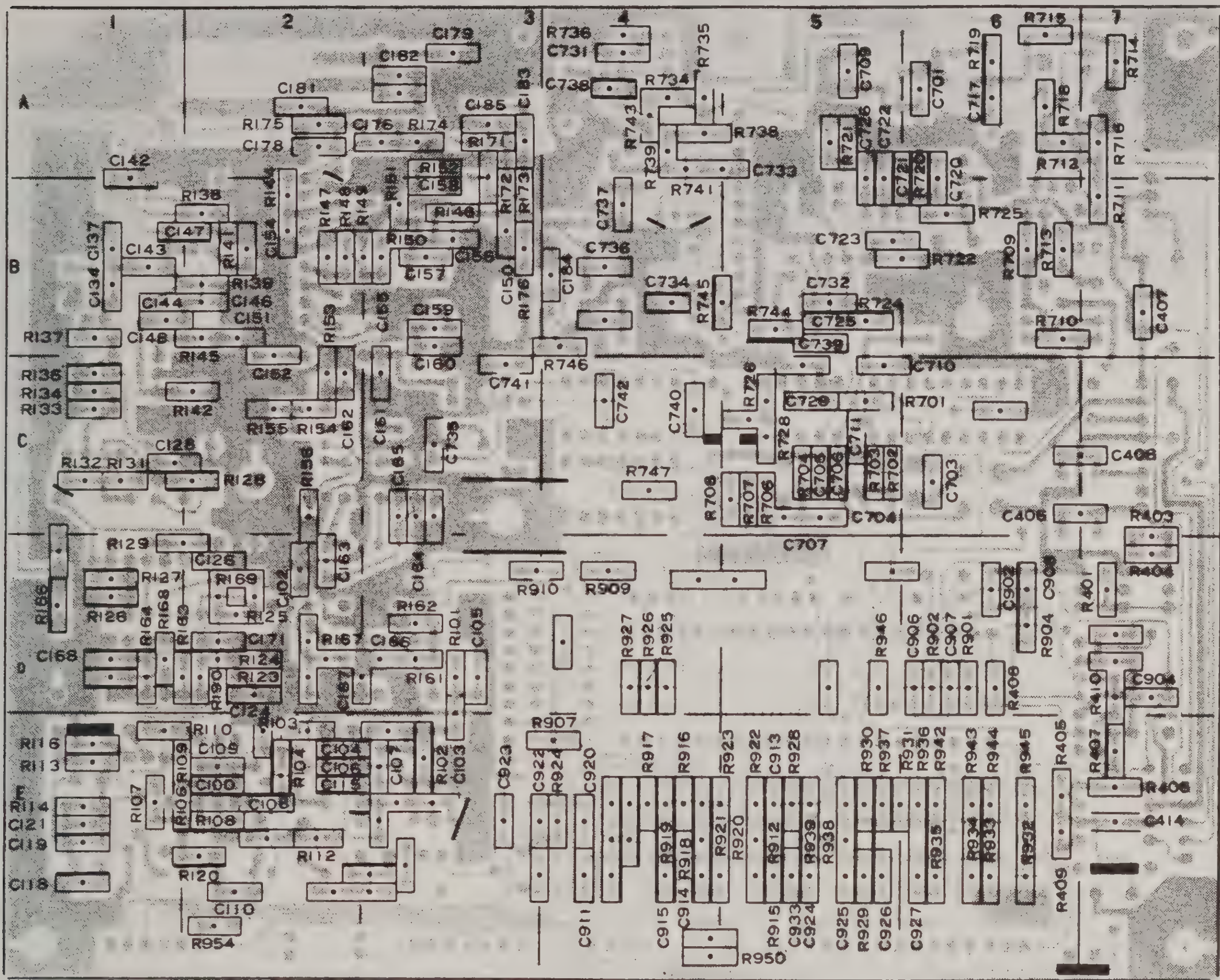

RX-154
Q201 2SK125
Q202 2SK125
Q204 2SA673C
Q203 2SC1906
Q205 2SC458C
Q251 2SC535B
Q252 2SC458C
Q255 2SC458C
Q256 2SC458C
Q257 2SC458C
Q259 2SK117BL
Q260 2SC458C
Q261 2SC458C
IC251 MC3357P
IC252 MB3712
FL251 21.4-15C
X251 20.945MHz
CFU-455E2
CFU-455D2
K201
P251 (CM202)
P358
J358
J352
J353
J354
J357
J351
J355
J356
TSQ SIG
TX TONE
TX TM
ALM
SQ SIG
TSQ MON
AF MUTE
HANGUP(G)
HANGUP
SP(G)
SP
SP(INT)
to P358
to OPTION BOARD

RECEIVER SCHEMATIC DIAGRAM



TRANSMITTER PC BOARD (TOP VIEW)





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A
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C
D
E
C179
C182
C181
R175
C176
R174
C178
C185
C183
R171
C142
R138
C147
C137
C134
C143
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R101
C105
R164
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R163
C168
C171
R124
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R157
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R161
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C911
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C915
C914
R950
C709
C701
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C717
R715
R714
R716
R721
C726
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C720
R712
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R711
R725
C723
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C732
R744
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R724
C739
C407
R710
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R701
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R728
C711
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C903
R904
R401
R946
C906
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R408
C904
R410
R922
C913
R928
R930
R937
R931
R936
R942
R943
R944
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R405
R407
R406
C414
R912
R939
R938
R935
R934
R933
R932
R409
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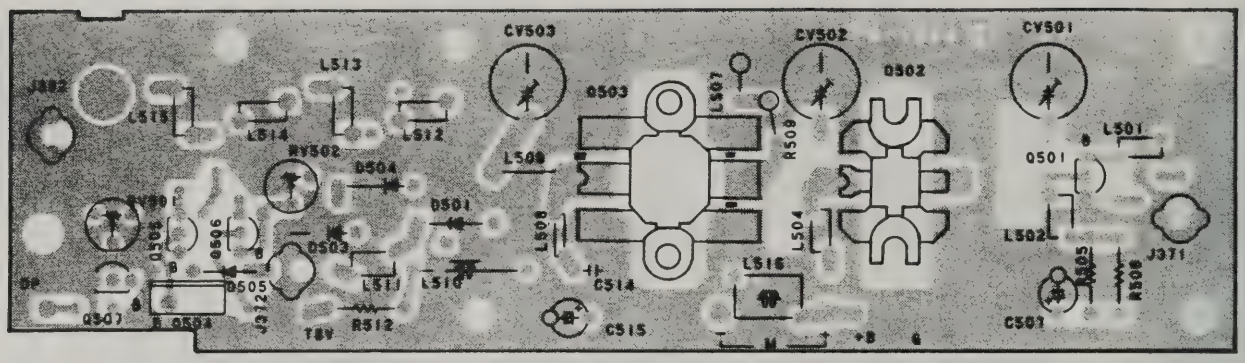
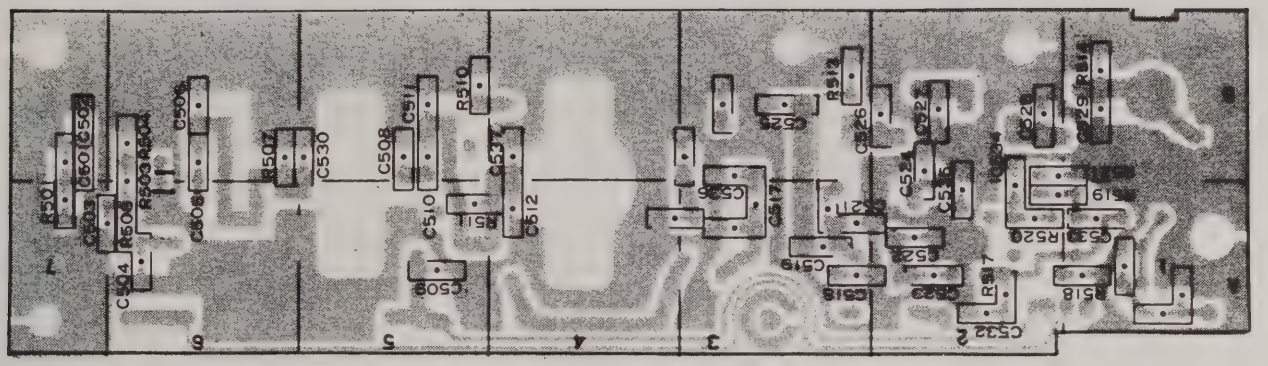
C924
C925
R929
C926
C927

PA PC BOARD (TOP VIEW)

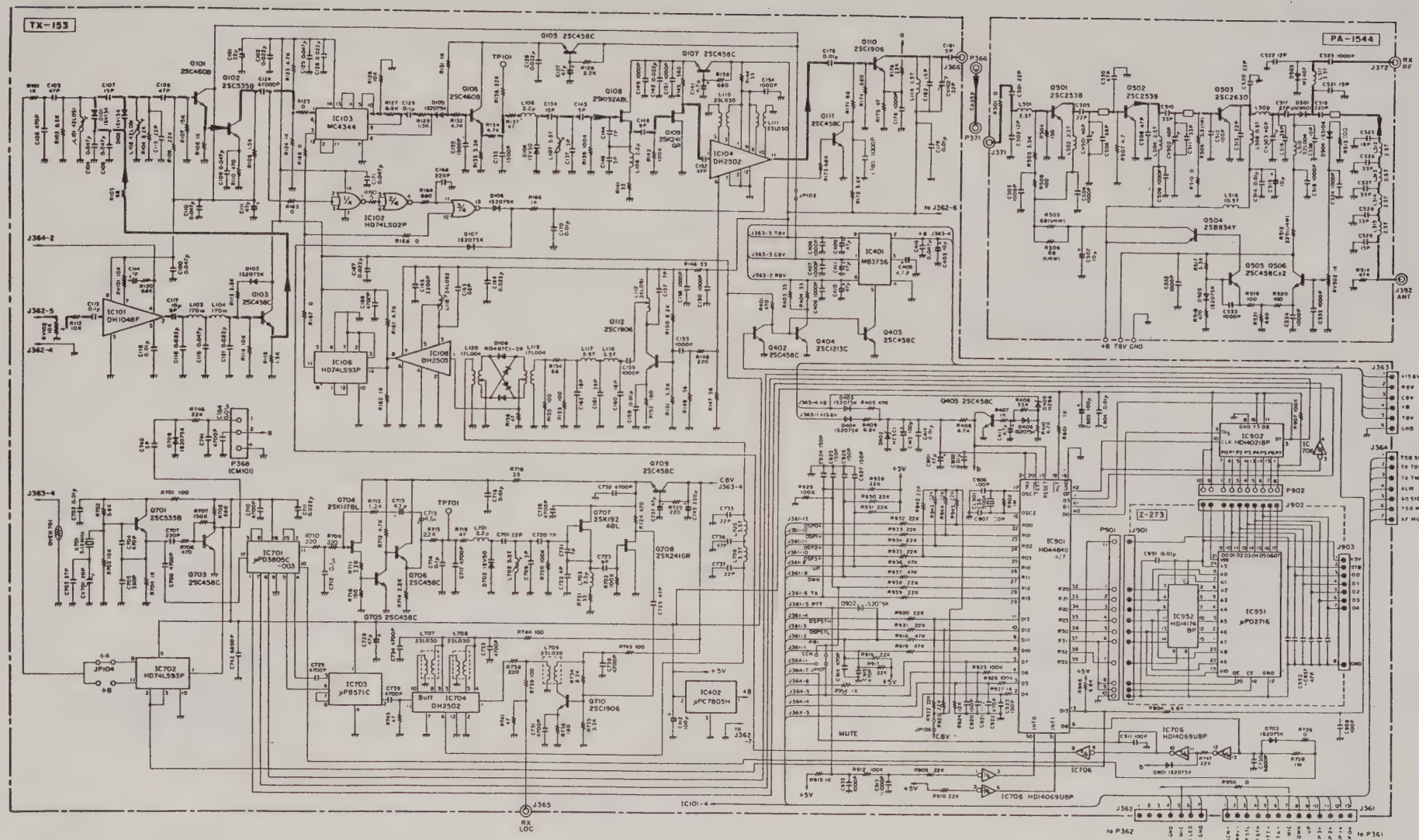


PA PC BOARD (BOTTOM VIEW)



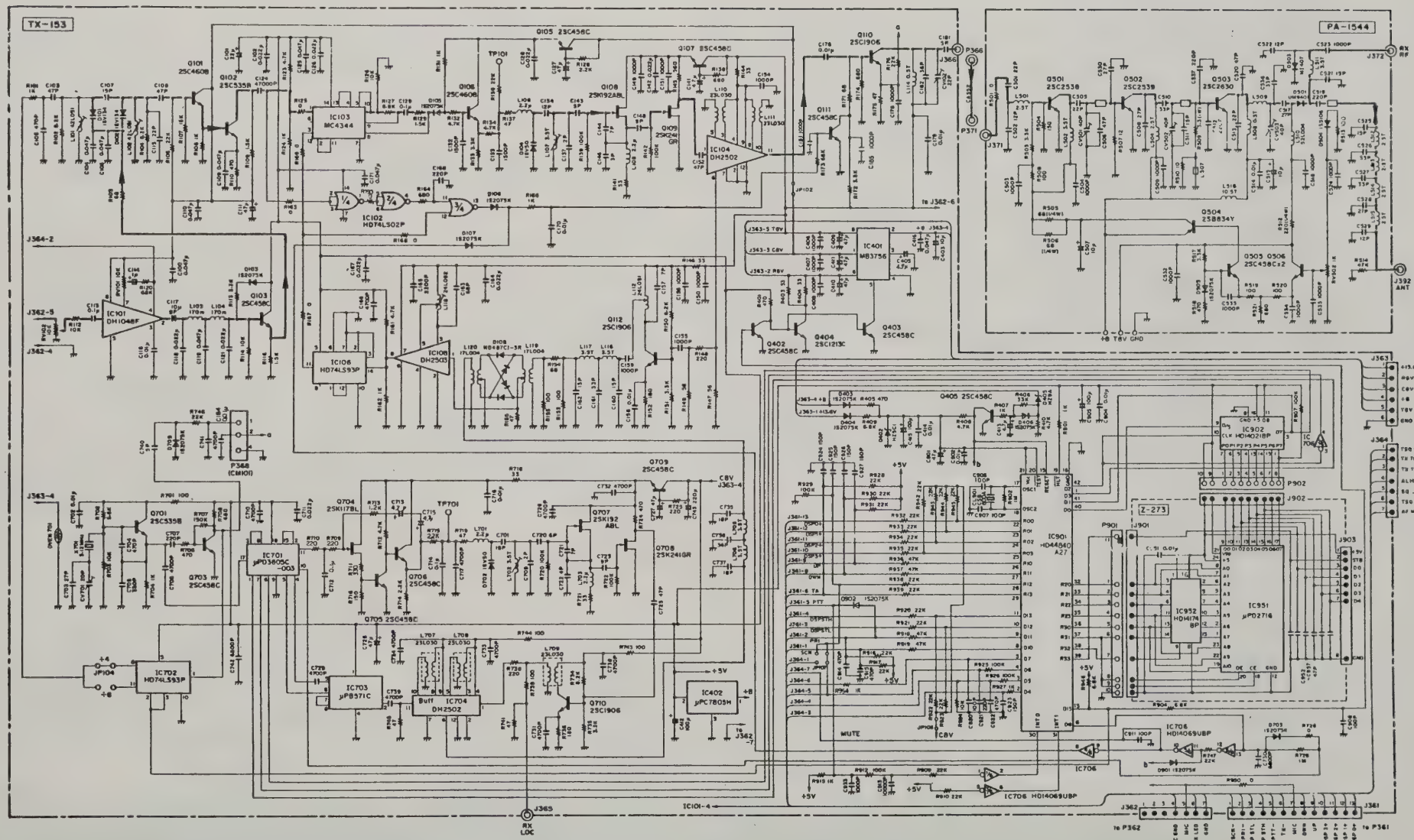
TRANSMITTER SCHEMATIC DIAGRAM

70-340A/440A

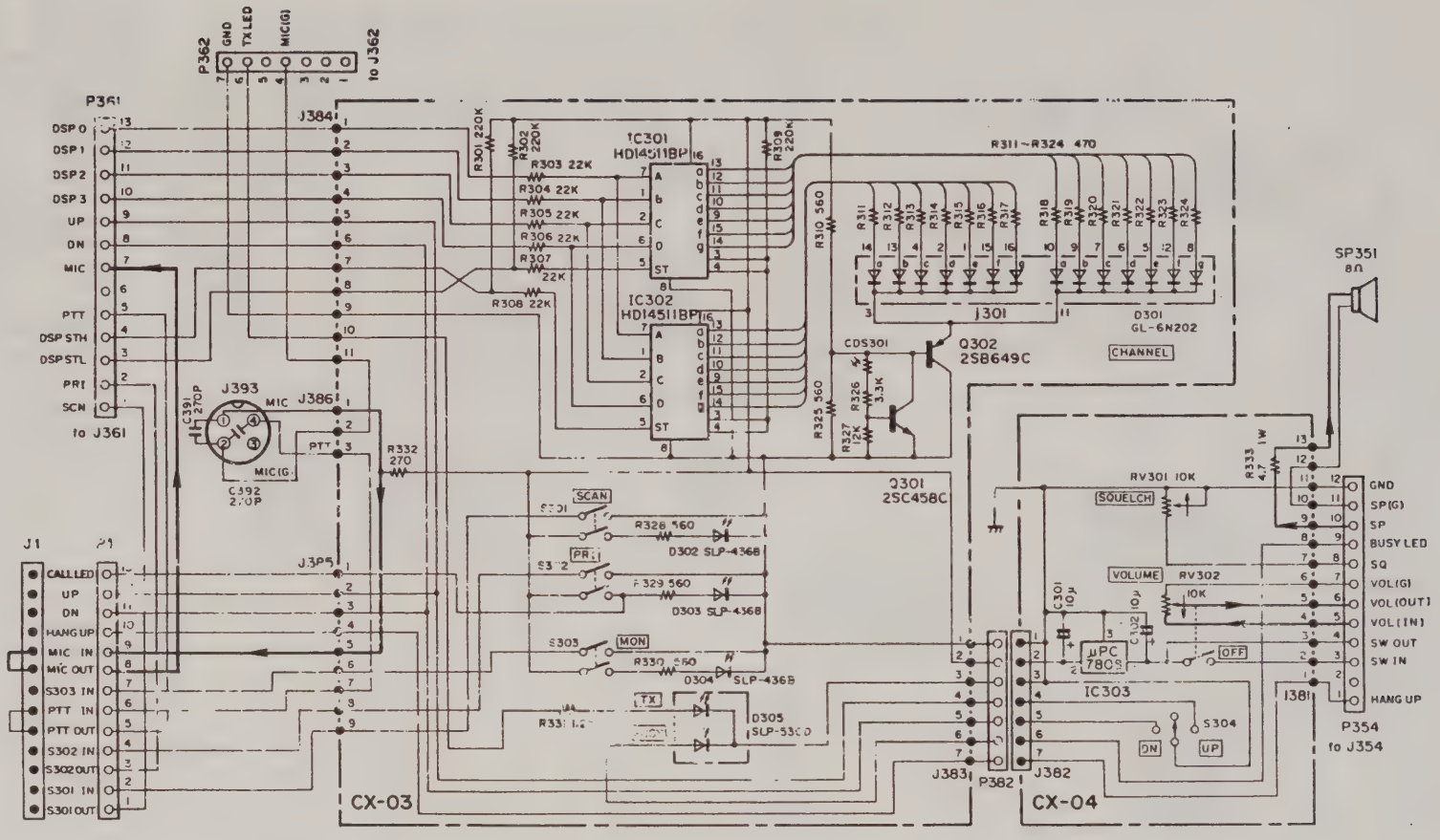


TRANSMITTER SCHEMATIC DIAGRAM

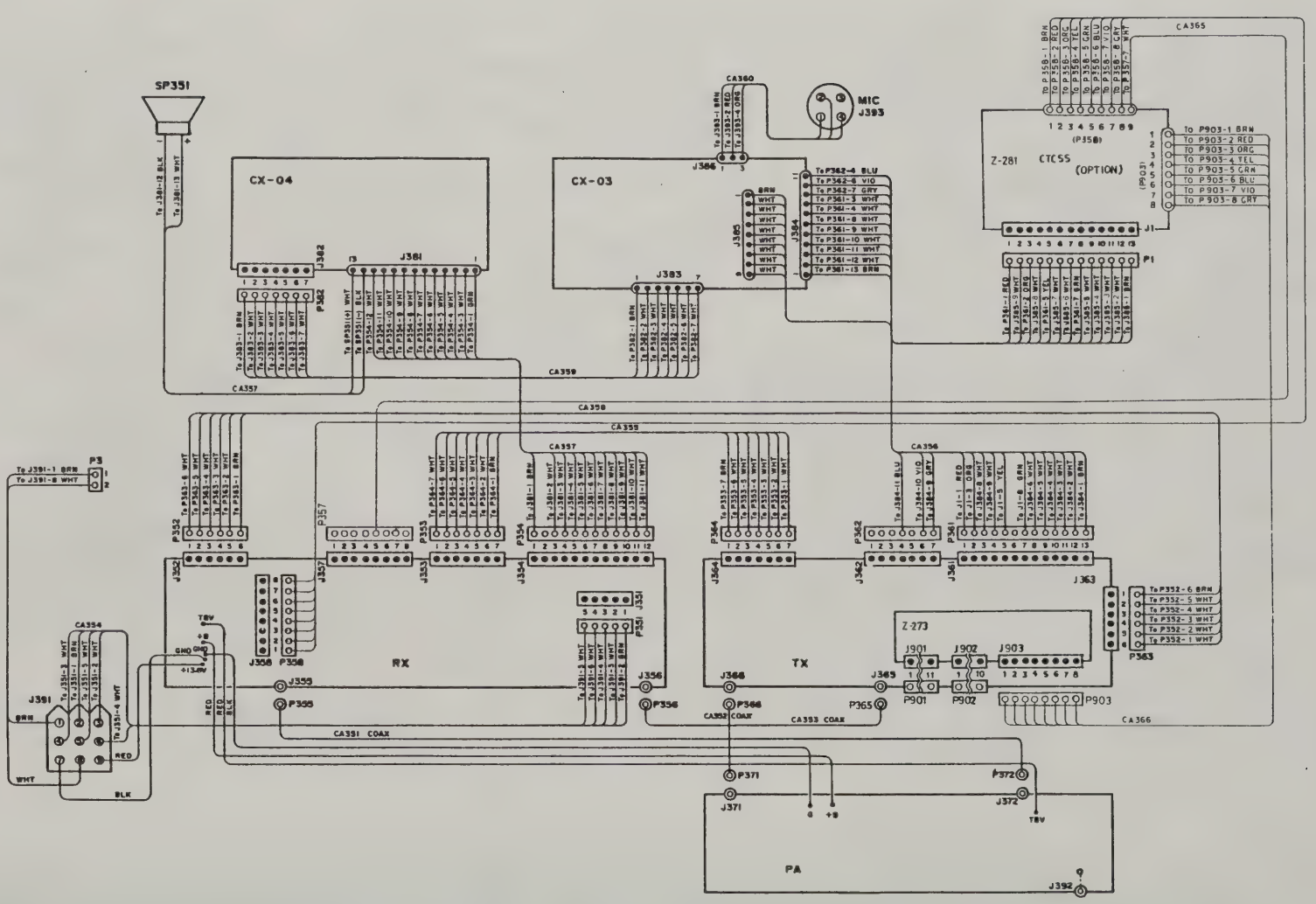
70-340B/440B



Fold Out

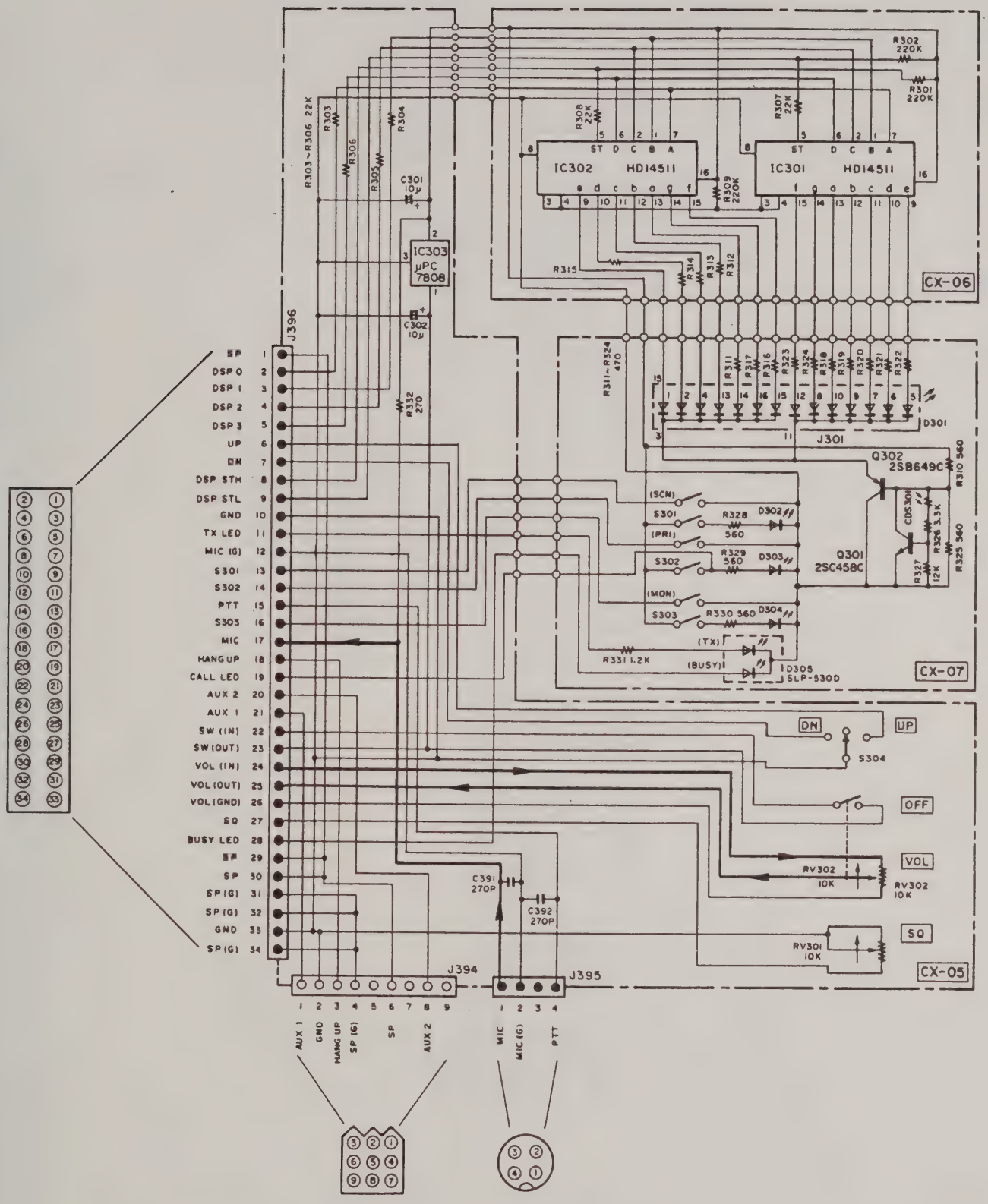

P362
GND
TX LED
MIC(G)
to J362
P361
DSP 0
DSP 1
DSP 2
DSP 3
UP
DN
MIC
PTT
DSP STH
DSP STL
PRI
SCN
to J361
J384
J386
J393
MIC
MIC(G)
PTT
C391 270P
C392 270P
R332 270
R301 220K
R302 220K
R303 22K
R304 22K
R305 22K
R306 22K
R307 22K
R308 22K
R309 220K
IC301 HD14511BP
IC302 HD14511BP
R310 560
R311~R324 470
J301
D301 GL-6N202
CHANNEL
CDS301
Q302 2SB649C
R325 560
R326 3.3K
R327 12K
Q301 2SC458C
SP351 8Ω
R333 4.7 1W
RV301 10K
SQUELCH
VOLUME
RV302 10K
C301 10μ
C302 10μ
μPC 7805
IC303
OFF
S304
DN
UP
J381
P354
to J354
GND
SP(G)
SP
BUSY LED
SQ
VOL(G)
VOL(OUT)
VOL(IN)
SW OUT
SW IN
HANG UP
J1
P1
CALL LED
UP
DN
HANG UP
MIC IN
MIC OUT
S303 IN
PTT IN
PTT OUT
S302 IN
S302 OUT
S301 IN
S301 OUT
J385
SCAN
S301
R328 560
D302 SLP-436B
PRI
S302
R329 560
D303 SLP-436B
S303
MON
R330 560
D304 SLP-436B
TX
R331
D305 SLP-530D
J383
P382
J382
CX-03
CX-04

PC BOARD INTER-CONNECT DIAGRAM



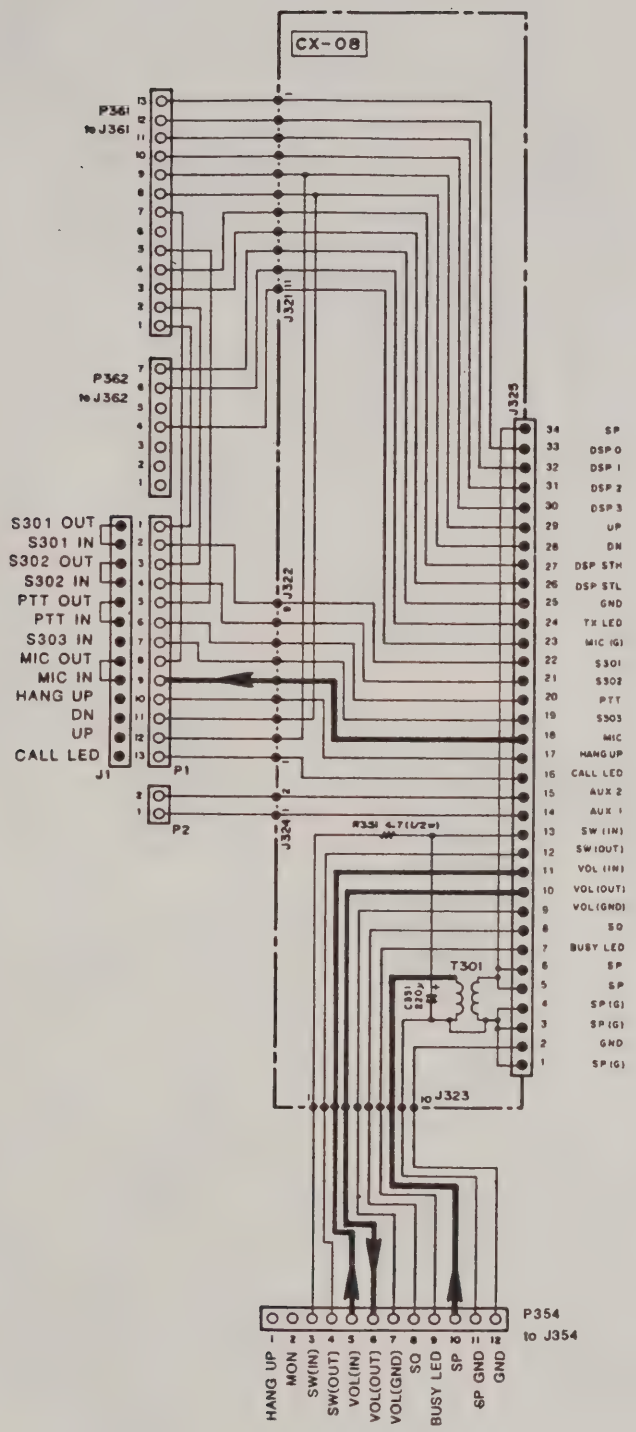
Fold Out

CONTROL HEAD SCHEMATIC DIAGRAM



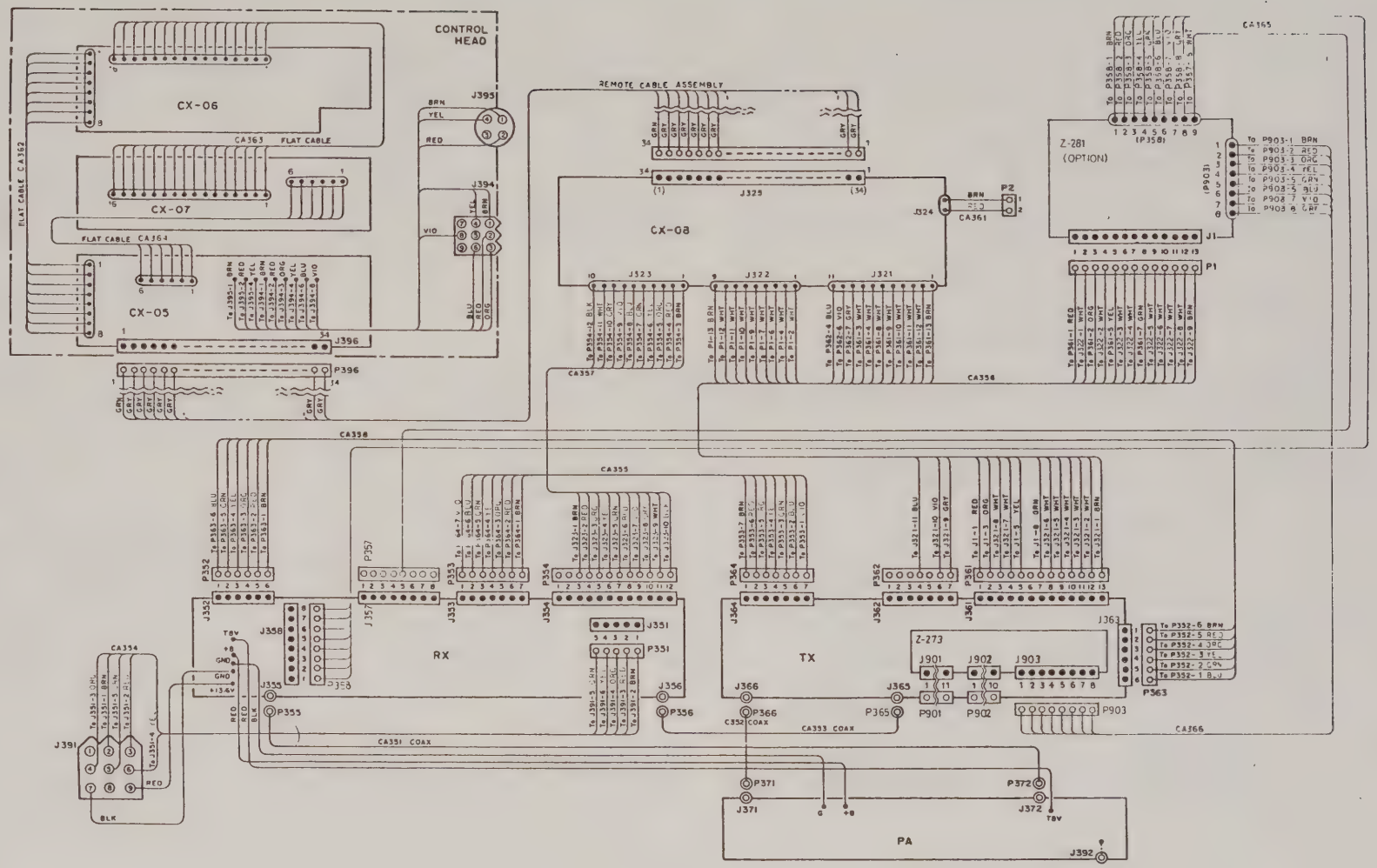
CONTROL INTERFACE SCHEMATIC DIAGRAM

70-440



PC BOARD INTER-CONNECT DIAGRAM

70-440A/B



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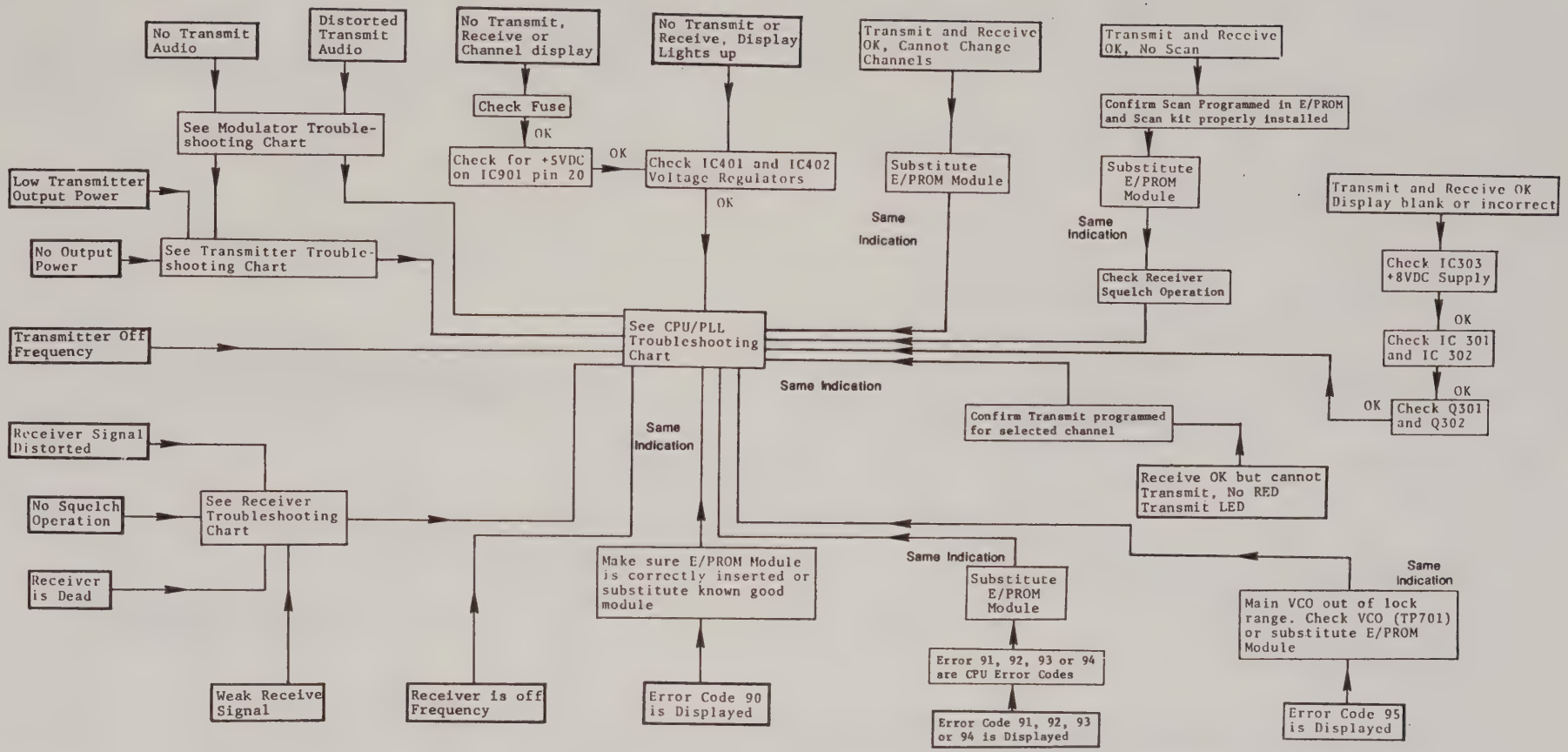
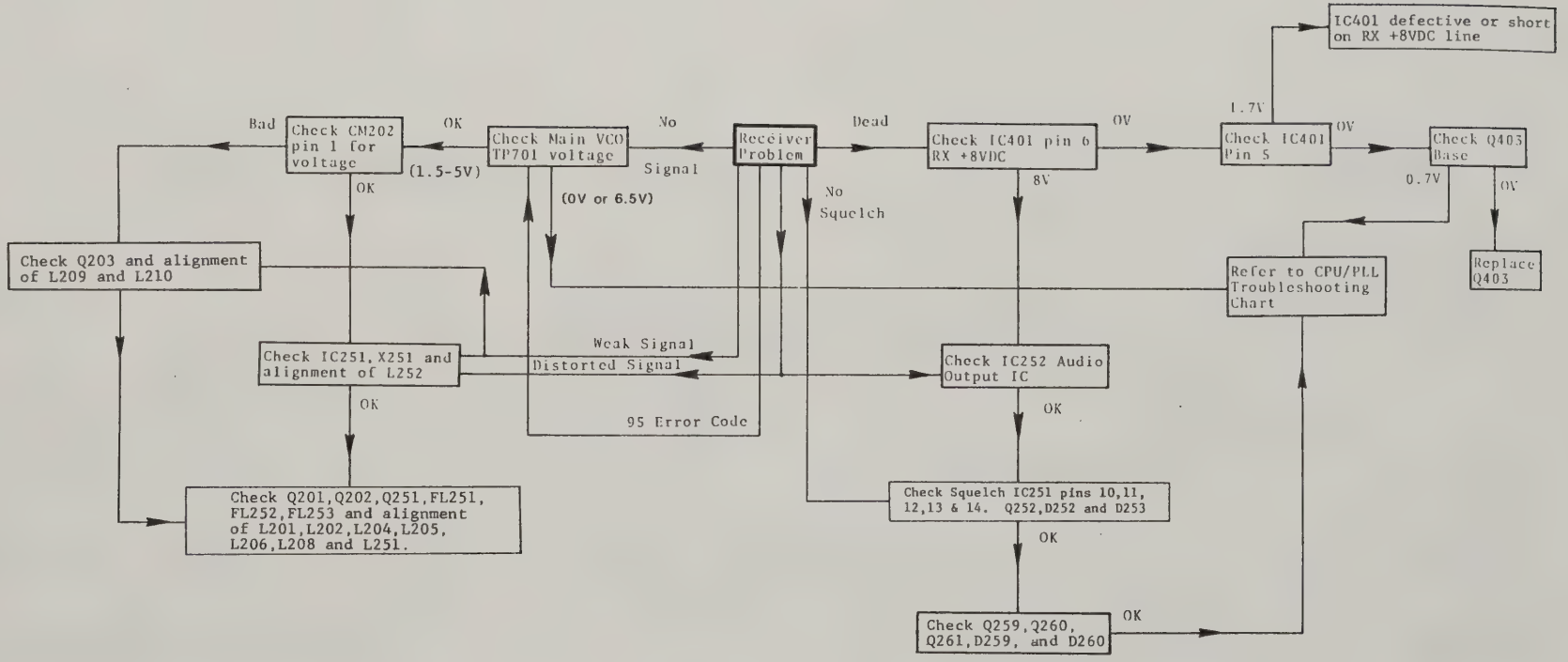
GENERAL TROUBLESHOOTING CHART



RECEIVER TROUBLESHOOTING CHART

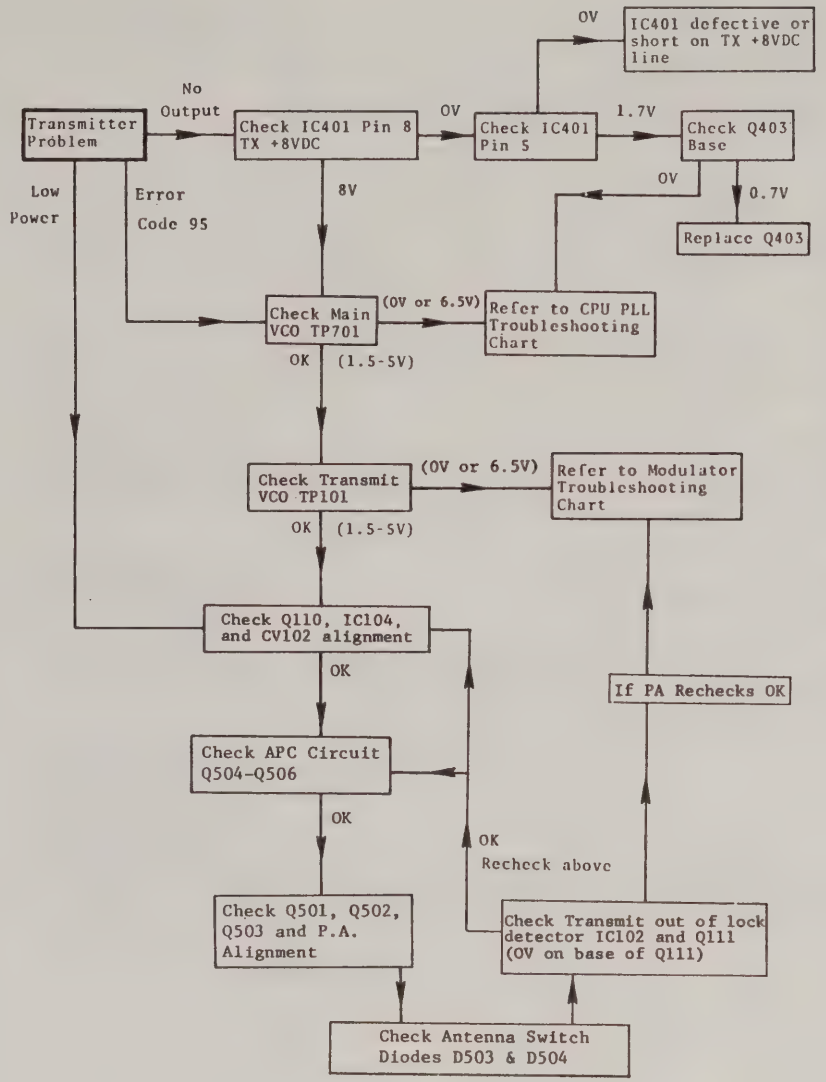
70-340/440



FOLD OUT →

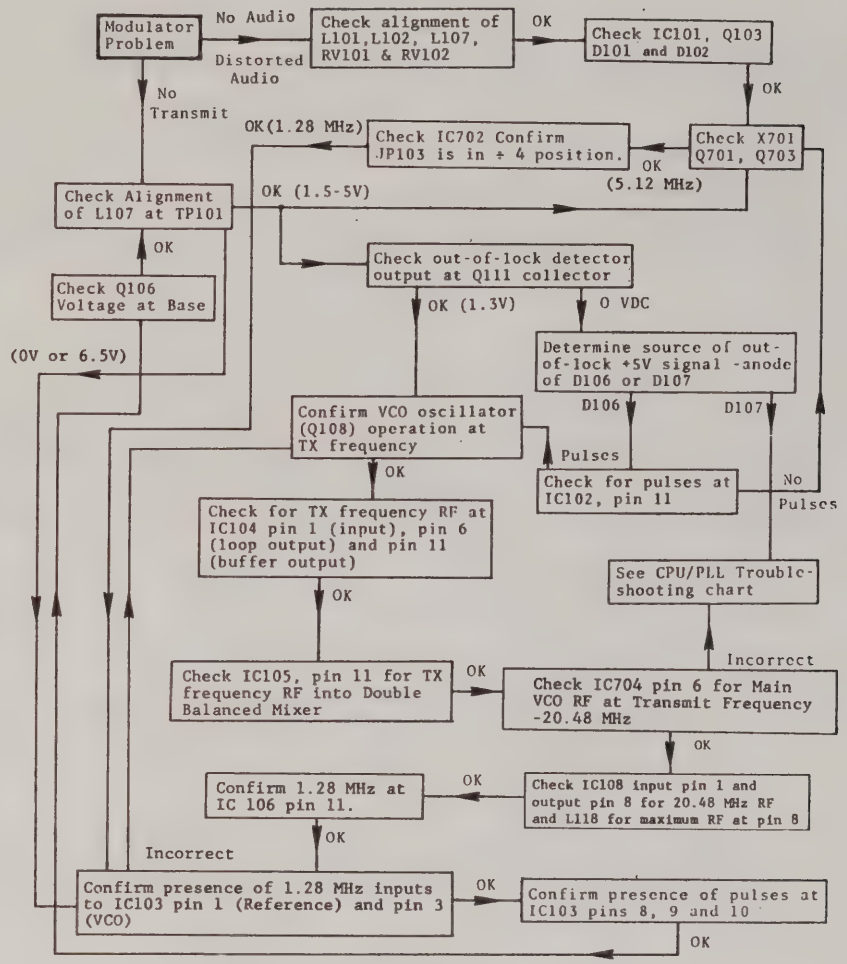
TRANSMITTER TROUBLESHOOTING CHART

70-340/440

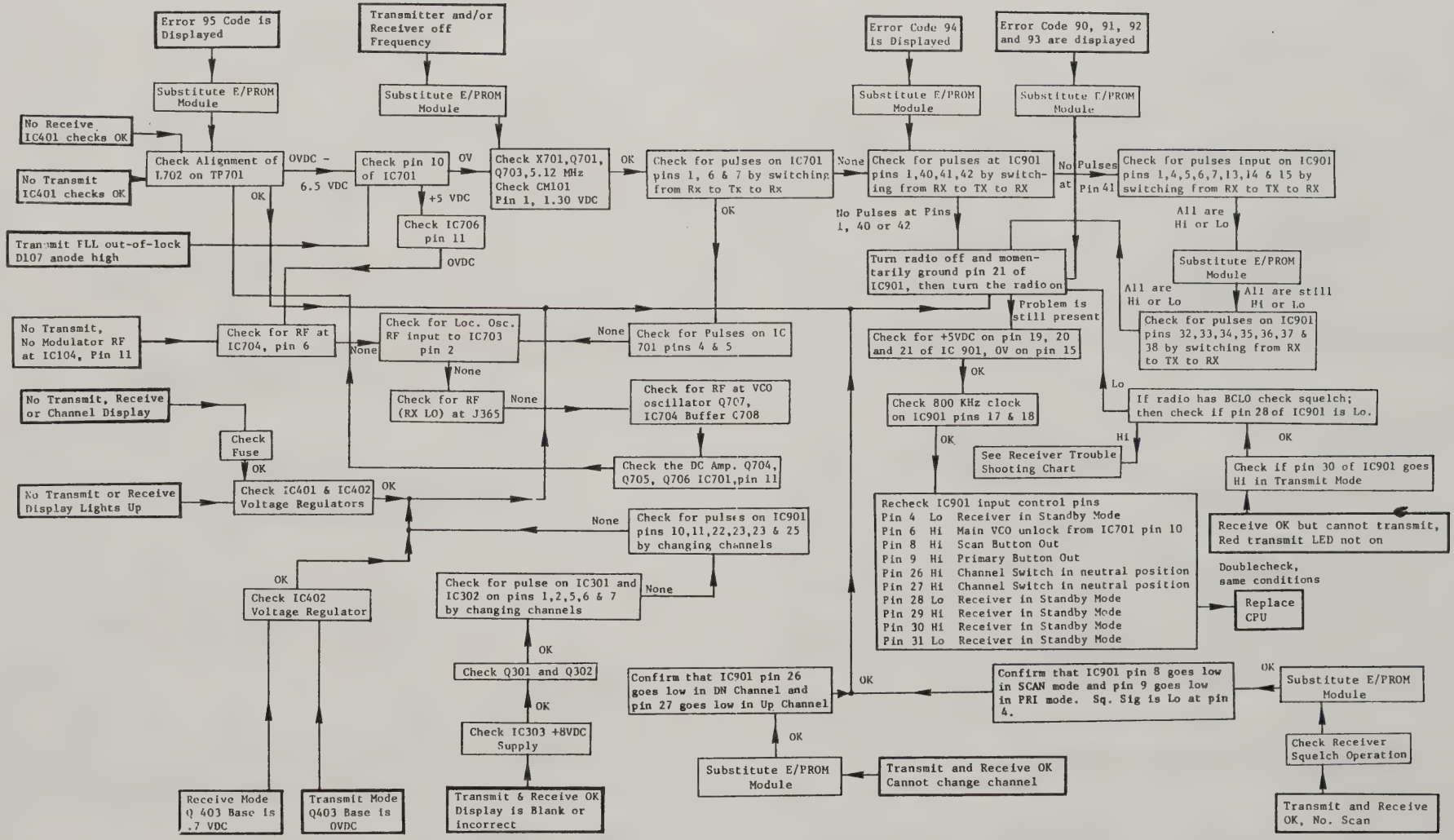


MODULATOR TROUBLESHOOTING CHART

70-340/440



CPU/PLL TROUBLESHOOTING CHART



FOLD OUT

TRANSISTORS

REF. NO.	DESCRIPTION	MODE	BASE	COLLECTOR	EMITTER	FUNCTION
Q101	2SC460B	TX	3.2	8.0	2.5	Buffer
Q102	2SC535B	TX	2.5	3.2	1.8	Buffer
Q103	2SC458C	TX	3.2	5.0	2.5	AF Buffer
Q105	2SC458C	TX	7.9	8.0	7.3	Power Line Filter
Q106	2SC460B	TX	2.3--7.0	7.3	1.6--6.3	Buffer
Q107	2SC458C	TX	7.9	8.0	7.3	Power Line Filter
Q110	2SC1906	TX	1.2	8.0	0.5	Pre Driver
Q111	2SC458C	TX	.1	1.35	0	Pre Driver Control
Q112	2SC1906	TX	1.9	7.6	1.35	Buffer
Q203	2SC1906	RX	0.6	6.0	0	1st Local Amplifier
Q204	2SA673C	RX	13.0	11.5	13.6	Power Regulator
Q205	2SC458C	RX	8.0	13.0	7.4	Power Control
Q251	2SC535B	RX	0.7	3.8	0	1st IF Amplifier
Q252	2SC458C SQ ON 2SC458C SQ OFF	RX RX	2.1 1.9	3.4 5	1.5 1.6	Noise Amplifier
Q255	2SC458C	RX	0	2.0	0	Sq. Switch
Q256	2SC458C	RX	0	7.4	0	Sq. Switch
Q257	2SC458C	RX	3.5	8.0	2.8	AF Pre Amplifier
Q260	2SC458C	RX	0.6	0.06	0	Sq. Switch
Q261	2SC458C SQ ON 2SC458C SQ OFF	RX RX	0.02 0	0.1 4.7	0 0	Sq. Switch
Q301	2SC458C 2SC458C	TX RX	.3-.7 .3-.7	1.8-4.0 1.8-4.0	0 0	Dimmer Control
Q302	2SB649C 2SB649C	TX RX	1.6-4.0 1.6-4.0	0 0	2.1-4.6 2.1-4.6	Dimmer Control
Q402	2SC458C	TX RX	0 0.7	0.7 0	0 0	Power Control
Q403	2SC458C	TX RX	0.7 0	0 2.0	0 0	Power Switch
Q404	2SC1213C	TX RX	0.7 0	0 8	0 0	Power Control
Q405	2SC458C	TX RX	0.6 0.6	0 0	0 0	Reset (MCPU)
Q501	2SC2438	TX	0.1	3--8	0	Pre Driver
Q502	2SC2539	TX	---	13.6	0	Driver
Q503	2SC2630	TX	---	13.6	0	RF Power Amp.
Q504	2SB834Y	TX	12.9	3--8	13.6	APC
Q505	2SC458C	TX	1.6	12.9	1.1	APC Amp.
Q506	2SC458C	TX	1.6--1.9	8.0	1.2	APC Amp.

TRANSISTORS (cont)

REF. NO.	DESCRIPTION	MODE	BASE	COLLECTOR	EMITTER	FUNCTION
Q701	2SC535B	TX RX	2.9 2.9	4.5 4.5	2.4 2.4	OSC (RX SYN)
Q703	2SC458C	TX RX	0.7 0.7	2.8 2.8	0 0	Buffer
Q705	2SC458C	TX RX	0.6 0.6	5.0 5.0	0 0	Loop Filter (RX Syn.)
Q706	2SC458C	TX RX	5.0 5.0	7.3 7.3	4.35 4.35	Loop Filter (RX Syn.)
Q709	2SC458C	TX RX	8.2 8.2	8.2 8.2	7.4 7.4	Power Line Filter
Q710	2SC1906	TX RX	1.9 1.9	7.3 7.3	1.4 1.4	Buffer

F.E.T'S

REF. NO.	DESCRIPTION	MODE	GATE	DRAIN	SOURCE	FUNCTION
Q108	2SK192A BL	TX	0	7.3	0.3	VCO (TX PLL)
Q109	2SK241GR	TX	0	2.9	0	Buffer
Q201	2SK125	RX	0	10.5	2.5	Front End Amp.
Q202	2SK125	RX	0	11.0	2.5	1st Mixer
Q259	2SK117BL SQ.OPN. 2SK117BL SQ.CLS.	RX RX	3.3 0	3.2 3.2	3.3 3.3	AF Switch
Q704	2SK117BL	TX RX	3.3 3.3	7.3 7.3	3.5 3.5	Loop Filter (RX Syn)
Q707	2SK192ABL	TX RX	0 0	7.4 7.4	0.3 0.3	VCO (RX Syn)
Q708	2SK241GR	TX RX	0 0	3.0 3.0	0.6 0.6	Buffer

DIGITAL IC

REF. NO.	DESCRIPTION	PIN NO.	+ V VOLTAGE	GND PIN NO.	FUNCTION:
IC 102	HD74LS02P	14	5	7	Nor Gates
IC 103	MC4344	14	5	7	Phase Detector
IC 106	HD74LS93P	5	5	10	4 Bit Binary Counter
IC 301	HD14511BP	16	8	8	Led Driver
IC 302	HD14511BP	16	8	8	Led Driver
IC 701	uPD3805C	18	5	9	PLL
IC 702	HD74LS93P	5	5	10	4 Bit Binary Counter
IC 703	uPB571C	1	5	4	Pre Scaler (Rx Syn)
IC 706	HD14069uPB	14	5	7	Buffer
IC 901	HD44840A27	20/21	5	16	CPU
IC 902	HD14021BP	16	5	8	Date Shifter (Rx Syn)
IC 951	uPD2716D	24	5	12	Read Only Memory
IC 952	HD14174BP	16	5	8	Data Buffer

ANALOG IC

REF.NO.	DESCRIPTION	MODE	PIN No.1	PIN No.2	PIN No.3	PIN No.4	PIN No.5	PIN No.6	PIN No.7	PIN No.8	PIN No.9	PIN No.10	PIN No.11	PIN No.12	PIN 13	PIN 14	PIN 15	PIN 16	FUNCTION
IC 101	DH 1048	TX	--	3.8	4.5	3.8	0	--	4.5	8	--	--	4.5	--					IDC
IC 104	DH 2502	TX	0	0	0	7.5	7.5	0	0	0	7.5	7.5	0	0					BUFFER
IC 108	DH 2503	TX	0	0	7.5	0	7.5	0	7.5	1.55	--	--	--	--					BUFFER
IC 251	MC3357P	SQUELCH CLSD. RX	7.6	7.1	7.6	7.6	1.0	1.0	1.0	7.5	3.7	1.9	1.9	.8	0	1.4	0	2.0	
		OPEN RX	7.6	7.1	7.6	7.6	1.0	1.0	1.0	7.5	3.7	1.9	1.9	0.2	7.0	0	0	2.0	2nd IF AMP
IC 252	MB 3712	RX	7.0	13.8	13.0	0	--	--	0.6	--	--	--	--	--					AF PWR AMP
IC 303	uPC7808H	TX	13.8	8.0	0	--	--	--	--	--	--	--	--	--					
		RX	13.8	8.0	0	--	--	--	--	--	--	--	--	--					POWER REGULATOR
IC 401	MB 3756	TX	8.0	13.6	8.0	0	0	0	0	8	--	--	--	--					
		RX	8.0	13.6	8.0	0	1.7	8	0	0	--	--	--	--					POWER REGULATOR
IC 402	uPC7805H		13.8	0	4.9														POWER REGULATOR
IC 704	DH2502	RX	0	0	6.8	6.8	0	0	0	6.8	6.8	0	0	0					BUFFER

MICROCOMPUTER (IC 901) PIN OUT DESCRIPTION

PIN NO.	PIN NAME	INPUT OUTPUT	SIGNAL NAME	FUNCTION
1	D3	OUT	DSTB+	Strobe for serial data to synthesizer
2	D4	OUT	TXTM-	Signalling option control (TX: LOW, RX: HIGH)
3	D5	OUT	ALM-	Alert (2KHz Tone)
4	D6	IN	SQSIG+	Squelch Signal (Busy; High)
5	D7	IN	TSQMON-	Tone/Monitor detect (low)
		OUT	TSQMON-	Scan hold status (NSQ Hold; Low)
6	D8	IN	PLCL-	Synthesizer Unlock: LOW (input)
		OUT	PLCL-	Audiomute & TX Inhibit: LOW (output)
7	D9	OUT	VCOCNT	VCO Band Switch High Frequency Range:LOW
8	D10	IN	SCN-	Scan Switch (on:LOW)
9	D11	IN	PRI-	Pri Switch (on: LOW)
10	D12	OUT	DSPSTL-	Display Data Ones Digit Strobe
11	D13	OUT	DSPSTH-	Display Data Tens Digit Strobe
12	D14	IN	ALBH-	Band Select (A:LOW, B:HIGH)
13	D15	OUT	TXDL	TX/RX Control (Tx:LOW Rx:HIGH)
14	NC	-	- - -	No Connection
15	RESET	-	- - -	General Reset (Reset: HIGH)
16	GND	-	- - -	Ground
17	OSC1			Clock Oscillator (800 KHZ ±5%)
18	OSC2			Clock Oscillator (800 KHZ ±5%)
19	HLT	-	- - -	Standby Mode Control (Standby: LOW)
20	TEST	-	- - -	Not Used (HIGH)
21	Vcc	-	- - -	Power Supply (+5V±10%
22	R00	OUT	DSP0+	LED Display Data (HIGH: 6 to 8V, LOW: 0 to 2V)
23	R01	OUT	DSP1+	LED Display Data (HIGH: 6 to 8V, LOW: 0 to 2V)
24	R02	OUT	DSP2+	LED Display Data (HIGH: 6 to 8V, LOW: 0 to 2V)
25	R03	OUT	DSP3+	LED Display Data (HIGH: 6 to 8V, LOW: 0 to 2V)
26	R10	IN	UP-	Channel Up Switch (ON:LOW)
27	R11	IN	DWN-	Channel Down Switch (ON:LOW)
28	R12	IN	INH+	PTT Inhibit (Inhibit: HIGH)
29	R13	IN	TA-	Wideband/Standard Select (WIDE:LOW)
30	INT0	IN	PTT INT+	PTT Switch (PTT: HIGH)
31	INT1	IN	- - -	Not Used
32	R20	OUT	RMA0+	E/PROM ADDRESS DATA
33	R21	OUT	RMA1+	RMA5+ is also used as the E/PROM ENABLE SIGNAL
34	R22	OUT	RMA2+	" " " " " " " " "
35	R23	OUT	RMA3+	" " " " " " " " "
36	R30	OUT	RMA4+	" " " " " " " " "
37	R31	OUT	RMA5+	" " " " " " " " "
38	R32	OUT	ASTB+	Strobe for E/PROM address data latch
39	R33	OUT	AUXSTB+	Strobe for AUX.DATA (Signalling Option Board)
40	D0	OUT	PSST+	Strobe for E/PROM DATA OUTPUT TO SHIFT REGISTER
41	D1	IN	CHDT+	Serial data from Shift Register
42	D2	OUT	DCLK	Clock for CHDT+

HIGH: 3.5 to 5V, LOW: 0 to 1.5V

Measure with high input impedance meter or oscilloscope

CHIP COMPONENT IDENTIFICATION

Chip components used in Midland SYN-TECH transceivers can be identified as follows:

COLOR	COMPONENT TYPE
Black	Metal Film Resistor
White with value marking	Metal Film Resistor
Light Brown	Ceramic Capacitor
Green	Ceramic Capacitor
White (no marking)	Ceramic Capacitor

Resistor value marking is as follows:

1st two digits - significant digits
3rd digit - number of added zeros

Example: 105 = 10 00000 = 1M Ohm

CHIP COMPONENT REMOVAL/REPLACEMENT

NOTE: Temperature of soldering iron must be maintained at 600-700°F.

COMPONENT REMOVAL

1. Place solder iron tip directly on component in order to melt solder and glue as shown in figure #1 & #2. Remove component with tweezers or long nose pliers.

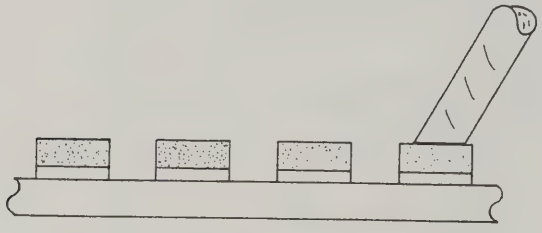


FIG. #1

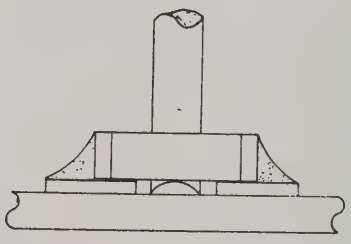


FIG. #2

2. Completely remove old solder from PC board, using a desoldering tool. Application of a small amount of flux will greatly aid in the removal of old solder.

CHIP COMPONENT REPLACEMENT

3. After component has been removed and PC pattern cleaned, apply a small amount of solder on PC pattern and let cool, as shown in figure #3.

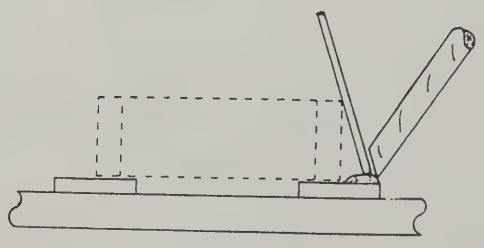


FIG. #3

CHIP COMPONENT REPLACEMENT (CONTINUED)

4. Insert new component and apply soldering iron tip to PC pattern as shown in figures 4, 5, 6 and 7.

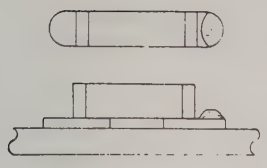


FIG. #4

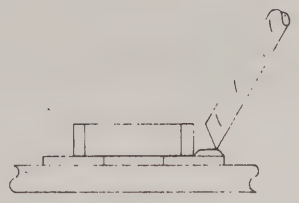


FIG. #5

FIG. #6

FIG. #7

CAUTION: As patterns and components are close to each other, extreme care must be exercised when soldering, as not to damage components or bridge PC pattern paths. High soldering iron temperatures can cause component damage. DO NOT apply the soldering iron tip to a new component during installation.

IC COMPONENT REMOVAL/REPLACEMENT

COMPONENT REMOVAL:

Extreme care must be exercised when removing and replacing defective transistors and IC's. Keep in mind that copper foil is employed on both sides of the printed circuit board. IC's and transistors may be removed from the circuit for testing. If IC's are to be removed from the circuit intact and unharmed, an IC desoldering tip attached to a soldering iron should be used. This tip will melt solder on all pin connections simulateously and the IC may be pulled from the PC board.

A solder suction tool or braided desoldering wick may be used to remove the solder, freeing one pin at a time. Carefully and thoroughly remove solder from all IC pins until the IC can be removed without resistance. When removing transistors for testing, use needle nose or clamping type seizing pliers that will act as a heatsink on the transistor leads. If a transistor or IC is defective, it may be cut from the leads and removed. The leads may be unsoldered and removed one at a time.

REPLACEMENT:

If it is necessary to bend IC leads, firmly hold and bend the lead with needle nose pliers. Make sure the leads are free from solder and are parallel to the IC body. Remove all solder from the holes in the PC board before attempting replacement. When replacing an IC or transistor on the PC board, make sure the component is properly orientated. Before soldering an IC, verify there is no AC voltage between the solder iron tip and common ground.

PC BOARD REMOVAL

TX/SYNTHESIZER PC BOARD

To remove the TX/Synthesizer PC board, remove the 8 Phillips head PC board mounting screws. Disconnect the 4 multi pin connectors at J363, J361, J362 and J364, located at the front of the board. Next disconnect the 2 Coaxial connectors at J365 and J366, located at the rear of the board. Slide the PC board to the rear of the radio to clear the front retaining tab, then pull up.

RX PC BOARD

To remove the RX PC board, remove the 5 Phillips head PC board mounting screws. Next disconnect the 5 multi pin connectors at J351, J354, J353, J352 and J358 located at the middle and front of the board. Disconnect the 2 Coaxial connectors at J356 and J355 located near the rear of the board. Slide the PC board to the rear of the radio to clear the front retaining tab and then pull up.

PA PC BOARD

To remove the PA PC board, loosen the 4 Phillips head screws (2 on each side) located at the outside rear of the unit. Tilt PA/heatsink downwards and remove the 2 Phillips head screws holding the PA cover and remove the cover. Remove the 10 Phillips head mounting screws holding the PC board and output transistors. Next unsolder the antenna connector which protrudes through the PC board on the left hand side. The antenna connector is soldered to the board at 3 connections. All solder must be removed from these connections before attempting to remove the board. Next disconnect the 2 coaxial connectors at J372 and J371 and pull up on board. The board will still be retained by power wiring but access to the rear of the PCB is possible.

IC 901 MICROCOMPUTER PIN OUT

LEVELS: (LOW = 0 - 1.5v) (HIGH = 3.5 - 5v)

Pin Number	Signal Name	Function
1	DSTB+	Output strobe from micro to IC701 Pin 1 for serial data transfer to synthesizer; CONDITION: Initial power up, channel change, scan stop, error code indication.
2	TXTM-	Output from micro to receiver BD. D259 cathode for receiver muting; CONDITION: Rx=High, Tx=Low.
3	ALM-	Output from micro of a 2KHz alert tone, to receiver BD. IC252 Pin 6 for speaker output; CONDITION: Error code indication, transmit time out timer, busy channel lock out, scan stop.
4	SQSIG+	Input to micro from squelch circuit Q255 collector; CONDITION: Busy channel, IC251 pin 14 goes low, collector of Q255 goes high (See Scan Theory of Operation)
5	TSQMON-	Input low level from tone BD./or monitor detect on receiver BD. Pin 2 of J354 or J357 Pin 5; CONDITION: CTCSS/CDCSS tone decode, monitor switch select. (See Scan Theory of Operation).
5	TSQMON-	Output low level from micro to open squelch gate; (See Scan Theory of Operation).
6	PLCL-	Input low level to micro from IC701 Pin 10, and output low level from micro to Q111 and J364 Pin 7 audio mute indicating synthesizer unlock; CONDITION: (See Modulator and Transmit PLL, microcomputor channel data transfer and manual channel change theory of operation)
7		NOT USED
8	SCN-	Input low level from front panel on J361 Pin 1 to micro for non-priority scan selection (Scan B)

IC 901 MICROCOMPUTER PIN OUT

LEVELS: (LOW 0 -1.5v) (HIGH = 3.5 -5v)

Pin Number	Signal Name	Function
9	PRI-	Input low level from front panel on J361 Pin 2 to micro for priority scan selection (Scan A)
10	DSPSTL-	Low level strobe output from micro to IC301 Pin 5 for display data ones digits.
11	DSPSTL-	Low level strobe output from micro to IC302 Pin 5 for display data tens digits.
12		NOT USED
13	TXDL	Output from micro to IC401 Pin 5 for Tx-8v and Rx-8v select. Tx=Low, Rx=High.
14		NO CONNECTION
15		High input pulse from Q405 resetting micro to an autotest mode at unit power up.
16		GROUND
17		800KHz Clock Oscillator
18		800KHz Clock Oscillator
19		Standby mode control; with power applied this line is high for normal micro functions, when this line is low (power off) micro functions are disabled.
20		NOT USED (HIGH)
21		VCC Power Supply +5v
22	DSPO+	Output from micro to IC301 and IC302 Pins 7, 1, 2, 6 for LED Display Data (High = 6 - 8v) (Low = 0 - 2v)
23	DSP1+	Same As DSPO+

IC 901 MICROCOMPUTER PIN OUT

LEVELS: (LOW 0 - 1.5v) (HIGH = 3.5 - 5v)

Pin Number	Signal Name	Function
24	DSP2+	Same As DSPO+
25	DSP3+	Same As DSPO+
26	UP-	Input low level from channel selector switch; CONDITION: Channel change up.
27	DWN-	Input low level from channel selector switch; CONDITION: Channel change down.
28	INH+	High level from receiver BD. for PTT Inhibit (See Busy Channel Lock Out Theory of Operation).
29		NOT USED
30	DTT IN7+	High input to micro from PTT mic switch.
31		NOT USED
32 - 37	RMA 0+ - RMA5+	Address data corresponding to the selected Rx channel which is strobed and latched into IC952 before being strobed into the shift register IC902. (See Microcomputer Channel Data Transfer Theory of Operation).
38	ASTB+	Output strobe for IC952 address data latch listed above.
39	AUXSTB+	Output strobe for Aux Data (Signaling Options Board-CTCSS) (See CTCSS Theory of Operation).
40	PSST+	Output strobe to IC902 shift register Pin 9. (See Microcomputer Channel Data Transfer Theory of Operation).
41	CHOT+	Serial data input from shift register IC902 Pin 3.
42	DCLK	Clock output signal to shift register IC902 Pin 10.